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Energimyndighetens titel på projektet – svenska Undersökning av modulära topologier för en STATCOM-enhet med utökad möjlighet för energiutbyte mellan fasbenen
Energimyndighetens titel på projektet – engelska Investigation of modular topologies for STATCOM application to facilitate energy exchange between the converter phase legs
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Förord

This PostDoc project has been sponsored by Energimyndigheten together with ABB Corporate Research Center (Västerås) and Chalmers Area of Advance. The project has been extensively discussed with industrial partners. Key researchers from ABB corporate research have been actively involved in the project. Furthermore, Prof. Jan R. Svensson, ABB Corporate Research and Adjunct Professor at Chalmers, has been extensively involved in supervision of the PostDoc.

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Sammanfattning

Installationen av förnybara energikällor ökar ständigt. Denna ökning av förnybar energi medför ett antal utmaningar för nätoperatörer såsom balansbehov mellan

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energiförsörjning och efterfrågan, systemstabilitet, elkvalitet och minskning av nätets kortslutningseffekt. Det är under detta scenario som kraftelektroniska baserade lösningar medför både möjligheter och utmaningar för en effektiv och säker drift av elnätet. Omriktare (Voltage Source Converter, VSC) för reaktiv effektkompensering, även kallad STATic COMpensator (STATCOM), är den mest lovande lösningen för att hantera utmaningar i samband med framtidens moderna och hållbara kraftsystem. Modular Multilevel Converters (MMCs) är de mest attraktiva VSC för STATCOM-applikationer. Bland MMCs anses idag Star (Y-) och Delta (Δ-) Cascaded H-bridge (CHB) vara den industriella standarden för STATCOM-applikationer. Både Y- och Δ-CHB har emellertid ett begränsat driftområde under vissa obalanserade förhållanden, vilket begränsar förmågan hos dessa två konfigurationer att hantera kraftsystemets framtida krav. Syftet med detta projekt är att undersöka alternativa konfigurationer av MMC, såsom hybridomvandlare och Double-Y MMC, för STATCOM-applikation. Projektets huvudfokus ligger på förmågan hos de undersökta omvandlarna att utbyta energi mellan omvandlarens fasben, vilket underlättar dess drift i obalanserade nät och samtidigt utöka omriktarens driftsområde jämfört med den mer traditionella CHB konfigurationen. Systemflexibilitet, liksom dimensionering och antal nödvändiga komponenter kommer att vara nyckelfaktorer för det slutliga valet av topologi.

Projektet genomförs i tre delar. Den första delen ägnas åt den gemensamma utmaningen bland MMC-topologierna, som är den individuella kondensatorens spänningsbalansering vid nollströmsläge. Med fokus på Y-CHB föreslås en ny metod för att övervinna detta problem. Den föreslagna metoden är baserad på modulering av DC-ledspänningarna. Resultaten visar effektiviteten hos den föreslagna metoden vid balansering av kondensatorens spänningar när ingen ström utväxlas med elnätet. Den föreslagna metoden kan användas för valfri MMC. Den andra delen är att undersöka hybridomvandlaren. En styrenhet för hybridomvandlaren för STATCOM-applikationer föreslås. Styrenheten maximerar omvandlarens driftområde. Resultaten visar att hybridomvandlaren möjliggör en effektiv utvidgning av omvandlarens driftområde, vilket indikerar att hybridomvandlaren kan vara en värdefull lösning för att övervinna Y-CHB begränsningar. Hybridomvandlaren tillåter dock inte helt täcka alla möjliga driftsförhållanden för omvandlaren vid drift under obalanserade förhållanden. Slutligen är den tredje delen att undersöka Double-Y MMC. Double-Y MMC har inte begräsningarna som förknippas med CHB och är därmed en värdefull topologi för den undersökta applikationen. Befintliga tillgängliga styrmetoder för Double-Y använder emellertid inte omvandlaren på det mest optimerade sättet. Detta projekt föreslår en ny styrstrategi för Double-Y MMC, som är baserad på noll-sekvens spänningsinjicering och ojämn strömfördelning mellan omvandlararmarna. Resultaten visar att den föreslagna strategin effektivt kan minska omvandlarens storlek jämfört med när de befintliga kontrollmetoderna för Double-Y används.

Enligt de erhållna resultaten framstår Double-Y MMC som den mest lämpliga omvandlingstopologin för nästa generation av STATCOM. De oanvända terminalerna på Double-Y kan också användas för integration av energilagring.

Nästa steg är att tillhandahålla en optimerad designriktlinje för Double-Y både med och utan energilagring.

Summary

The installation of renewable energy sources is constantly increasing. This increase in renewable energy brings a number of challenges for utilities and grid operators such as balance requirement between energy supply and demand, system stability, power quality and decrease of the short-circuit power of the grid. It is under this scenario that power-electronic based solutions represent both opportunities and challenges for an effective and secure operation of the electric power grid. Voltage Source Converters (VSC) for reactive power compensation, also named STATic COMpensator (STATCOM), are the promising solution to handle challenges associated with the modern and sustainable power system of future. Modular Multilevel Converters (MMCs) are the most attractive VSCs for STATCOM applications. Among MMCs, star (Y-) and delta (Δ-) Cascaded H-bridge (CHB) are today considered the industrial standard for STATCOM applications. However, both Y- and Δ-CHBs have a restricted operating range under certain unbalanced conditions, which limits the ability of these two configurations to handle the future demands of the power system. The aim of this project is to investigate alternative configurations of MMCs, such as hybrid converter and double-Y MMC, for STATCOM application. The main focus of the project is on the ability of the investigated converters to exchange energy between the converter phase-legs, thus facilitating its operation under unbalanced grids and at the same time extend the operating range of the converter as compared with the more traditional CHB configurations. System flexibility, as well as dimensioning and number of needed components will be key factors for the final topology selection.

The project is conducted in three parts. First part is dedicated to the common challenge among MMCs, which is the individual capacitor voltage balancing at zero-current mode. Focusing on the Y-CHB, a novel method to overcome this problem is proposed. The proposed method is based on modulation of the dc-link voltages. The results show the effectiveness of the proposed method in balancing the capacitors voltages when no current is exchanged with the grid. The proposed method can be used for any selected MMC. The second part is to investigate the hybrid converter. A controller for the hybrid converter for STATCOM applications is proposed. The controller maximizes the operating range of the converter. The results show that the hybrid converter allows to effectively extend the operating range of the converter, indicating that the hybrid converter can be a valuable solution to overcome the limitations of the Y-CHB. However, the hybrid converter does not allow to fully cover all possible operating conditions for the converter in case of operations under unbalanced conditions. Finally, the third part is to investigate the double-Y MMC. Double-Y MMC does not have the limits associated with the CHBs and is thereby a valuable topology for the investigated application. However, existing control approaches for the double-Y do not utilize the converter in the most optimized way. This project proposes a novel control strategy for the double-Y MMC, which is based on zero-sequence voltage injection and unequal current distribution between the converter arms. The results show that

the proposed strategy can effectively reduce the converter ratings as compared with the existing control approaches for the double-Y.

According to the obtained results, the double-Y MMC appears as the most suitable converter topology for the next generation of STATCOM. The unused terminals of the double-Y can also be used for energy storage integration. The next step is to provide an optimized design guideline for the double-Y both with and without energy storage.

Inledning/Bakgrund

Renewable energy sources play a significant role in the future of electric power system. In particular, wind and solar installations continue to increase as utilities and power providers are turning to cleaner, more sustainable and abundant sources of energy. As an example, the capacity of renewable generation in Sweden reached 52.6% of the total generation capacity since 2014, with a peak of about 10% of energy production from wind and solar in 2015 [1]. These numbers are constantly increasing. It is also reported that by year 2040, the generation capacity in Sweden should reach 100% renewables, with about 45% of the total generation capacity coming from wind and solar [2]. However, the future energy mix and the inherited intermittent nature of renewables brings a number of challenges for utilities and grid operators. The electric power grid is a very complex system that continuously requires a balance between energy supply and demand due to its inability to store energy. Adding variable sources of energy may greatly alter this critical balance. System stability and power quality issues can quickly emerge as soon as wind speed changes, or sun exposure varies throughout the day [3]. Furthermore, a large penetration of power-electronically controlled generation units might lead to a decrease of the short-circuit power of the grid, thus bringing possible stability issues in the future. It is under this scenario that power-electronic based solutions represent both opportunities and challenges for an effective and secure operation of the electric power grid.

The actual trend in the market clearly indicates that Voltage Source Converter (VSC) based power electronic controllers will be more and more utilized in the power systems, both for utility and industrial applications, thanks to the relatively small footprint, excellent dynamic performance and robustness in case of connection to weak grids. In the last years, extensive research has been addressed worldwide toward new VSC topologies, trying to achieve high-performance control together with system losses minimization. This is the driving force of several projects that have been initiated all around the world in the direction of Modular Multilevel Converters (MMC) applied to FACTS and HVDC systems [4]. Today, the MMC is considered as one of the most attractive topologies available for grid applications and in the recent years it has gained more and more attention both from the research community and the manufacturers [5]. Among the others, research on this topic is conducted in Canada [6], United Kingdom [7][8], Germany [9], France [10] and USA [11], to name a few.

In an MMC structure, each phase-leg of the converter is constituted by a number of modules (or cells) connected in series; each module can have a Half- or a Full-Bridge (HB or FB) structure. Among the MMCs family, the Cascaded H-Bridge (CHB) converter is the industrial standard for controllable reactive power compensators (also named STATic COMpensators, STATCOMs) [12]. For this converter topology, the phase legs can be connected either in delta (Δ) or in star (Y), depending on the specific application. In several works available in the literature, the Y-CHB is considered as the most suitable configuration for positive-sequence reactive power control, typically for voltage regulation purpose and, more in general, for utility applications; on the other hand, Δ-CHB is considered to be the best solution for applications where negative-sequence is required, as it is the case for industrial applications. The main disadvantage with CHB converters for grid applications is the lack of a common dc link and thereby the difficulty in exchanging energy between the phase legs. This leads to control and design challenges in case of operation under unbalanced grids, where control countermeasures must be taken in order to preserve the balancing of the capacitors, thus avoiding drifting of the dc-link voltages [13][14]. However, recent researches have shown that severe limitations exist when a CHB-based STATCOM is meant to be operated under unbalanced conditions [15]. In particular, it has been shown that the Y-CHB is sensitive to the ratio between the positive- and negative-sequence components of the current exchanged with the grid, while the Δ-CHB is sensitive to the ratio between the negative- and positive-sequence components of the voltage at the converter terminals. For both configurations, a singularity in the control solution for the voltage capacitor balancing exists when the above-mentioned ratios tend to unity. The existence of these singularities severely limits the application range of CHB-STATCOMs especially when the recent requirements from Transmission System Operators (TSOs) starts to demand negative-sequence injection capability for the converters connected to their grid [16]. This simply indicates that CHB is not the suitable topology for the next generation of STATCOM applications and that new solutions must be exploited and investigated.

This project will focus on proposing and investigating novel modular converter topologies aiming at facilitating the energy exchange between the converter's phase legs, thus allowing unbalance operation and energy storage integration. The main expected result from this project is detailed analysis of converter topologies, together with their control and modulation algorithms, suitable for operation under unbalanced grid conditions. System flexibility as well as dimensioning and number of needed components will be key factors for the final topology selection. The investigated topologies will be analyzed analytically, through dynamic simulations and in the laboratory.

Genomförande

The project has been conducted based on a pre-defined time plan that has been closely followed. Generally, a detailed theoretical analysis has been performed on the various issues and the results have been verified on a small-scale prototype in the laboratory. The results are provide by Ehsan Behrouzian (Postdoc at Chalmers), in cooperation with Prof. Massimo Bongiorno (project leader, Chalmers) and Prof.

Jan R. Svensson (ABB corporate research and Adjunct Professor at Chalmers). The most interesting results obtained from this project have been presented in various international conferences. The main method of result documentation is through publications in international conferences and journals, from which this report is based on. The list of publications resulting from the project can be found in the publication list of this report.

Resultat

In the following, the obtained results are presented in three parts. The first part is dedicated to a common challenge among all the MMCs, which is the individual capacitor voltage balancing at zero current mode (conference article I). The second part is dedicated to the investigation of the hybrid converter and its control (conference article II). Finally, the third part is dedicated to the double-Y MMC (conference article III and journal I). Note that the notation for each part might slightly differ from the others, as each part is a summary of a separate paper.

Part I. Individual capacitor voltage balancing

Several control techniques for the individual capacitor voltage balancing associated to MMCs has been presented in the literature. However, no specific solution for the individual capacitor voltage balancing especially when the converter is operating at zero-current mode is given so far. Therefore, it is of a high importance to find a robust solution for this problem first. At zero-current mode no power is exchanging between the converter and grid. The balancing algorithm requires information about the power direction for proper insertion of the different cells of the converter. If no power is exchanged, then the balancing algorithm will simply fail in providing a proper balancing. Focusing on the Y-CHB, the issue related to the capacitor voltage balancing at zero-current mode is highlighted in this part of the report and a novel method to overcome this problem is proposed. The proposed method is based on modulation of the dc-link voltages. The method provides a small amount of current flow during the zero-current mode operation. This current enables the sorting algorithm to provide an appropriate individual balancing. The simulation and experimental results show the effectiveness of the proposed method in balancing the capacitors voltages when no current is exchanged with the grid. Although the focus here is on the Y-CHB, the proposed method can be applied to any selected MMC topology.

I.1 Topology and control overview

Figure 1(a) shows the line-diagram of a Y-CHB. The control method (Figure 1 (b)) is implemented in the synchronous *dq*-frame, where the inner loop aims at controlling the converter output while the outer loops are to control the capacitor voltages at each phase and the exchanging reactive power. A Phase Locked Loop

(PLL) estimates the grid-voltage angle θ, used for grid synchronization and coordinate transformation.

The inner-current control loop, based on a PI regulator, generates the reference voltages for each phase. Since the *dq* frame is synchronized with the grid voltage, the quadrature component of the current is associated with the reactive power, while the direct component is associated with the active power. Therefore, the direct component can be used to compensate the STATCOM losses and regulate the dc-link voltage.

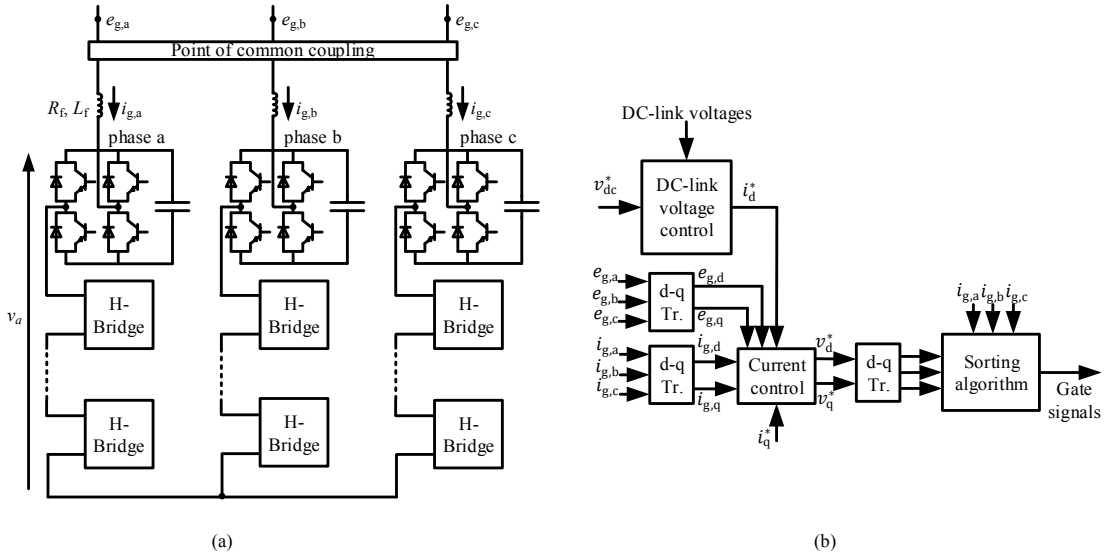

Figure 1 (a) Star-connected CHB-STATCOM, (b) control block

I.2 Zero-current operating mode

At zero current mode, where no current is exchanged between the converter and the grid, under ideal conditions the instantaneous current (constituted by the switching ripple only) should change its sign exactly in the middle of the control period. This provides equal charging and discharging areas for the capacitor, leading to a constant dc-link voltage. However, in practical applications this symmetry is typically not achieved, leading to slightly more charging or discharging area. Therefore, the dc-link voltages will not remain constant and diverge from their reference values. The conventional sorting approach will not be able to provide a proper balancing in this case, since the sorting approach inserts or bypasses the cells based on the current sign; as the current sign detected in the beginning of the control period is changed during the control period, the inserted cells capacitor voltages will deviate from the logic predicted by the sorting approach.

To highlight the problem at zero-current mode, the conventional sorting algorithm is applied to a 7-level Y-CHB-STATCOM implemented in PSCAD. The system parameters selected for the simulation are reported in Table 1. Figure 2 shows the obtained simulation results when using the conventional sorting algorithm. Figure 2 (a) shows the line current in phase *a*, while Figure 2 (b) shows the resulting dc-

link voltages in phase *a*. Similar behavior can be observed for the other phases. All figures are showing the measured quantities in per unit (pu). At t=0.9 s, the reactive current is changed from 0.5 pu peak to zero. As it can be observed, the conventional sorting algorithm is not able to provide proper individual cell balancing at zero-current mode.

Table 1 Circuit parameters in Figure 1

Rated apparent power	S	120 MVA, 1 pu
Nominal line to line rms voltage	V_s	33 kV, 1 pu
Filter inductance	L	4.3 mH, 0.15 pu
Filter resistor	R	0.136 Ω, 0.015 pu
DC bus voltage of each cell	V_{dc}	10.5 kV, 0.32 pu
Carrier frequency for PWM	f_c	3000 Hz
Grid frequency	f_0	50 Hz
Number of cells per phase	N	3
Capacitor size	C	4mF, 0.087 pu

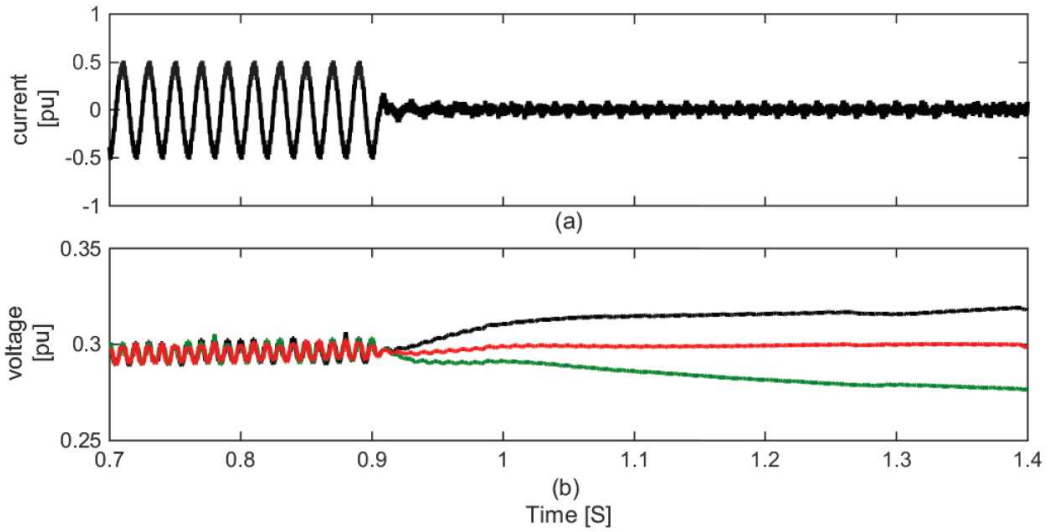

Figure 2 Sorting algorithm simulation results. (a) Line current, (b) Capacitor voltages

I.3 Proposed dc-link voltage modulation method

Since the problem with the individual dc-link balancing at zero-current mode is being the current very small, the dc-link voltage modulation method attempts to

increase the amplitude of the current at zero-current mode by exchanging a small amount of active current with the grid. Active current exchange can be achieved by allowing the capacitor voltages to gently increase and decrease around the desired reference value. To achieve this, a low-amplitude/low-frequency sinusoidal component can be added to the reference dc voltage once the converter operates at zero-current mode, thus forcing a small current exchange between the converter and the grid.

The amplitude of the sinusoidal component should not increase the dc-link voltage beyond the safety margin of the converter. Considering the fundamental component of the current only and neglecting the filter losses, with reference to Figure 1 the converter maximum and minimum voltages are calculated as

Equation 1

$$V = E_{\mathrm{g}} \pm X_{\mathrm{L}} I_{\mathrm{g,rated}}$$

where $I_{\mathrm{g,rated}}$ is the rated current of the converter, E_{g} is the rated grid voltage and X_{L} is the impedance of the filter inductance. According to (Equation 1) the dc-link voltage band for each cell of the Y-CHB with N number of cells per phase leg is located between a minimum and maximum value as

Equation 2

$$V_{\mathrm{dc}} = \frac{E_{\mathrm{g}} \pm X_{\mathrm{L}} I_{\mathrm{g,rated}}}{N}$$

The dc-link voltage reference can then be written as

Equation 3

$$v_{dc}^{*} = \begin{cases} v_{\mathrm{dc,0}}^{*} + v\cos(2\pi f_{\mathrm{d}} t) & i_q^{*} = 0 \\ v_{\mathrm{dc,n}}^{*} & i_q^{*} \neq 0 \end{cases}$$

where $v\cos(2\pi f_d \mathrm{t})$ is the sinusoidal component with amplitude of v and frequency of f_d; the zero-current mode is activated when $i_q^{*} = 0$. The required dc-link voltage at zero-current mode is equal to the middle of the dc-link voltage band calculated in (Equation 2). Therefore, $v_{\mathrm{dc,0}}^{*}$ and v in (Equation 3) should be selected so that the dc-link voltage oscillates between the maximum and the middle of the dc-link voltage band to avoid any over modulation. The voltage $v_{\mathrm{dc,0}}^{*}$ in (Equation 3) can be either designed for the maximum dc-link voltage level or it can be programmed to vary according to (Equation 2). The selection of f_d is dependent on the discharging time constant of the dc-link capacitors. It is recommended to select the period of the oscillations, $(\frac{1}{f_d})$, at least one decade larger than the capacitor's time, constant to ensure that the capacitor voltages will follow the reference voltage. This recommendation also ensures that the dc-link voltage controller will not impact the current-control loop, since the of the current-control loop bandwidth is typically much higher than f_d.

Since the capacitors require small amount of current to change their voltage level, the current resulting from the use of this technique is low and the measurement

noise and ripple may affect the proper sorting algorithm. Therefore, it is advisable to estimate the current for the sorting algorithm instead of using the measured signal. Since the reactive current during the zero-current mode is very small ($i_d \gg i_q$) and assuming a fast and precise current controller ($i_d^* \approx i_d$), it is possible to estimate the current in each phase of the star as

Equation 4

$$\hat{\imath}_{\mathrm{aY}} = \frac{\sqrt{2}}{\sqrt{3}} i_d^* \cos(\theta)\,, \hat{\imath}_{\mathrm{bY}} = \frac{\sqrt{2}}{\sqrt{3}} i_d^* \cos\left(\theta - \frac{2\pi}{3}\right), \hat{\imath}_{\mathrm{cY}} = \frac{\sqrt{2}}{\sqrt{3}} i_d^* \cos(\theta + \frac{2\pi}{3})$$

where the factor $\frac{\sqrt{2}}{\sqrt{3}}$ relates to the use of power invariant scaling for coordinate transformation and $\cos(\theta)$ is to make the current in phase with the grid voltage (since the current is mainly active current). Note that i_d^* is determined by the dc-link voltage control loop (see Figure 1). The current information required for the sorting algorithm can then be written as

Equation 5

$$i = \begin{cases} \text{estimated current from (Equation 4)} \\ \text{measured current} \end{cases}$$

According to (Equation 5), once the converter starts to operate at zero-current mode, the estimated currents of (Equation 4) are used in the sorting algorithm. For any other operating mode, the measured currents are used. It is of importance to stress that the estimated currents are only used in the sorting algorithm at zero-current mode. The current control will still use the measured currents in the feedback loop. The overall control block diagram with the proposed control algorithm at zero-current mode is shown in Figure 3.

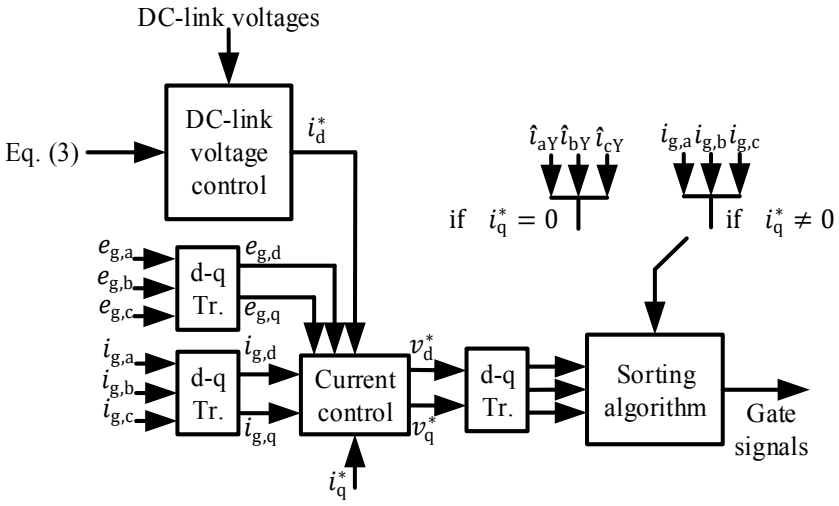

Figure 3 Overall control block diagram with proposed algorithm at zero-current mode

I.4 Simulation results

The proposed dc-link voltage modulation method is applied to the same simulation case study presented earlier. Based on the proposed algorithm, the DC-link voltage reference is defined as

Equation 6

$$v_{\mathrm{dc}}^{*}[\mathrm{pu}] = \begin{cases} 0.2961 + 0.0239\cos(2\pi 5t) & i_q^* = 0 \\ 0.32 & i_q^* \neq 0 \end{cases}$$

Note that the required dc-link voltage for the zero-current mode is equal to 0.2722 pu. Therefore, to keep the oscillations of the DC-link voltage between 0.2722 and 0.32 pu, $v_{\mathrm{dc},0}^{*}$ and v in (Equation 3) are selected as in (Equation 6). 5 Hz is selected for the frequency of the dc-link voltage oscillations.

Figure 4 shows the reactive and active currents together with the corresponding capacitor voltages when using the proposed dc-link voltage modulation technique. As it is shown in Figure 4 (a), the reference reactive current is set to -1 pu and is changed to 0 and 1 pu at t=0.5 s and t=1.5 s, respectively. Figure 4 (b) shows the reference active component of the current. It can be observed that once the dc-link modulation technique is activated, i_d^* starts to gently increase and decrease. This leads to a small amount of current flowing into the phase legs of the converter, which is used to provide the appropriate sorting algorithm. Figure 4 (c) shows the capacitor voltages when the measured currents are used in the sorting algorithm, while Figure 4 (d) shows the capacitor voltages when using the estimated currents. It can be observed that using the measured current in the sorting algorithm does not result in a perfect individual balancing while using the estimated currents leads to a proper balancing among the dc-link voltages. This is due to the fact that the current resulting from the proposed method is very small and the current ripples cause problem in appropriate sorting action.

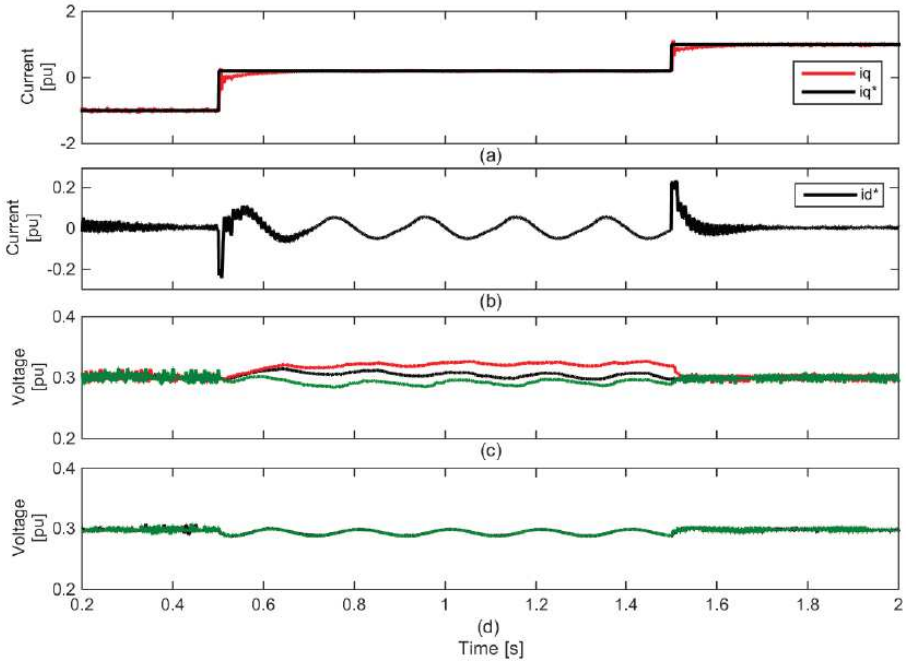

Figure 4 Simulation results with the proposed method. (a) Reactive component of the current and its reference, (b) Reference active component of the current, (c) Capacitor voltages in phase *a* by using measured current in the sorting algorithm (d) Capacitor voltage in phase *a* by using estimated current in the sorting algorithm

As the current introduced by the proposed method is small, measurement noise can also affect the proper sorting action. To evaluate the robustness of the proposed method, measurement noise (random data with 5% of the nominal values) are added to the measured data. The same simulation as in Figure 4 is implemented and the results are shown in Figure 5. It can be observed that proposed method is still able to provide the correct balancing.

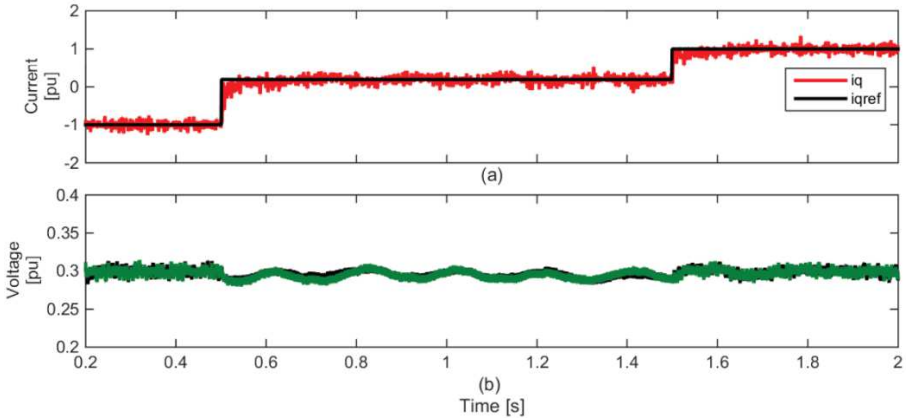

Figure 5 Simulation results of phase *a* in presence of noise, delay, dead-time and voltage drop. (a) Reference and actual reactive component of current, (b) Capacitor voltages

As STATCOM might be operated in distorted grids, it can be of interest to investigate the effectiveness of the proposed method in case of presence of harmonics in the PCC voltage. In this case, the resulting capacitor voltages are

shown in Figure 6. The reference reactive current is the same as in Figure 4 (a). It can be observed that in this case the individual balancing is not perfect. Ideally the grid voltage harmonics should not affect the performance of the controller as grid voltage feed-forward is used in the inner current controller. The feed-forward term allows a perfect voltage compensation thus blocking any current harmonic flow into the converter. But since the controller is implemented in discrete time, delays due to discretization and computational time in the control computer result in a phase shift between the actual and the feed-forwarded grid voltage. These phase shifts are typically compensated for the fundamental voltage component only, leading to a harmonic current flow between the VSC and the grid.

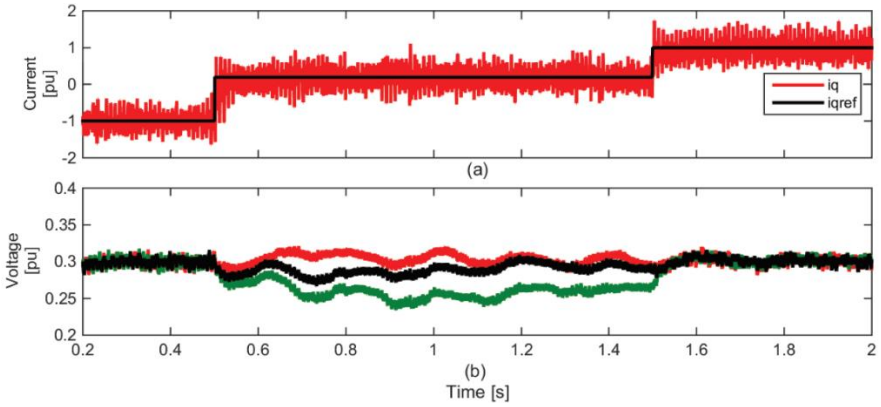

Figure 6 Simulation results of phase *a* in presence of grid voltage harmonics. (a) Reference and actual reactive component of current, (b) capacitor voltages

The presence of the harmonic currents has an impact on the decision taken by the sorting algorithm. This is due to the fact that for the investigated case the harmonics have an amplitude that is higher than the fundamental component. In order to avoid this effect and at the same time increase the system performance, when the converter is operated under distorted grids the amplitude of the oscillations introduced in the dc-link voltage are increased, which leads to increase the amplitude of the fundamental current component. For the considered case, the dc-link voltage reference can be set as

Equation 7

$$v_{\mathrm{dc}}^{*}[\mathrm{pu}] = \begin{cases} 0.3 + 0.03\cos(2\pi 5t) & i_q^{*} = 0 \\ 0.32 & i_q^{*} \neq 0 \end{cases}$$

This indicates that carefulness must be taken in selecting the amplitude of the oscillations when the converter has to be operated under distorted conditions, in order to avoid that the dc-link voltage exceeds the ratings of the cell. Figure 7 shows the simulation results with the modified dc-link voltage reference. It can be observed that under this condition the proposed algorithm allows to keep the capacitor voltage balanced.

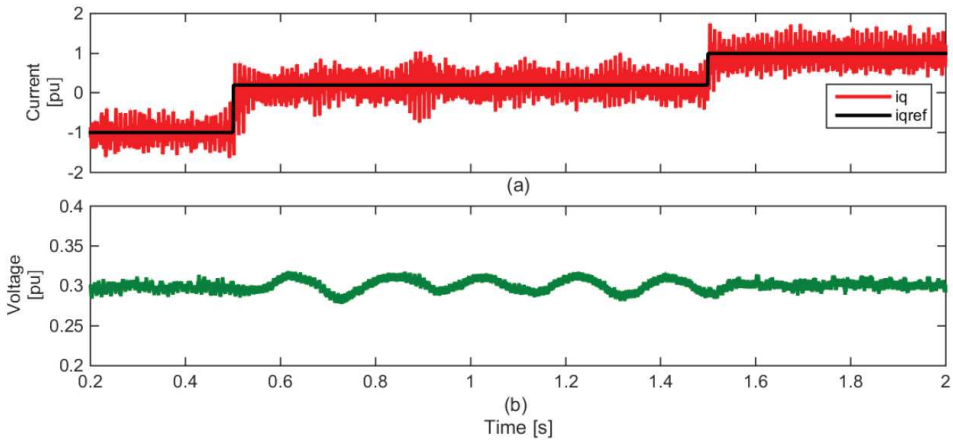

Figure 7 Simulation results of phase *a* in presence of grid voltage harmonics and the modified dc-link voltage reference

I.5 Experimental results

A down scaled laboratory set-up of the Y-CHB-STATCOM shown in Figure 8, with the system parameters reported in Table 2, is used to verify the proposed method. As the parameters of the experimental set-up differ from the simulated model, the reference dc-link voltage is recalculated here. Based on the system parameters, the maximum required dc-link voltage is equal as 0.354 pu. The required dc-link voltage for the zero-current mode is equal to 0.271 pu. Therefore, to keep the oscillations of the dc-link voltage between 0.271 and 0.354 pu, $v^*_{\mathrm{dc},0}$ and v in (Equation 3) are chosen to be 0.312 and 0.0006 pu. 5 Hz is selected for the frequency of the DC-link voltage oscillations.

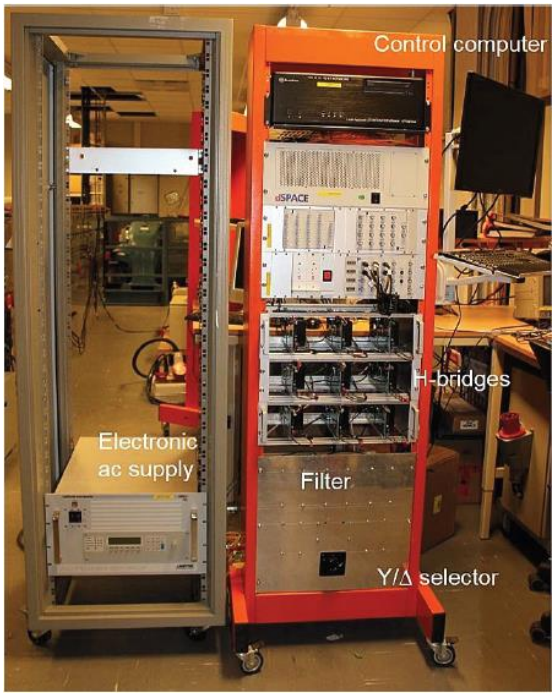

Figure 8 Picture of the laboratory

Table 2 Experimental set-up parameters

Rated apparent power	S	1.5 kVA
Nominal line to line rms voltage	V_s	173.2 V
Filter inductance	L	15 mH
Filter resistor	R	1.4 Ω
DC bus voltage of each cell	V_{dc}	62 V
Carrier frequency for PWM	f_c	3000 Hz
Grid frequency	f_0	50 Hz
Number of cells per phase	N	3
Capacitor size	C	4mF

Equation 8

$$v_{\mathrm{dc}}^{*}[\mathrm{pu}] = \begin{cases} 0.312 + 0.0006\cos(2\pi 5t) & i_q^* = 0 \\ 0.354 & i_q^* \neq 0 \end{cases}$$

Figure 9 shows the obtained experimental results. Figure 9 (a) shows the reference and actual reactive component of the current. Figure 9 (b) shows the reference active component of the current (i_d^*). Figure 9 (c) shows the dc-link voltages in phase *a* when the measured currents are used in the sorting algorithm and Figure 9 (d) shows the experimental results when the estimated currents are used instead. The reactive current is set to 1 pu until t=1.5 s and is then set to zero from t=1.5 s to t=7.5 s and to -1 pu from t=7.5 s to t=8.5 s. It can be observed that when the converter starts to operate at zero-current mode, the dc-link voltage modulation technique is activated, which leads to small oscillation in i_d^*. It can also be observed that the sorting algorithm provides a proper balancing when estimated current are used while it fails when using the measured currents, confirming the simulation results.

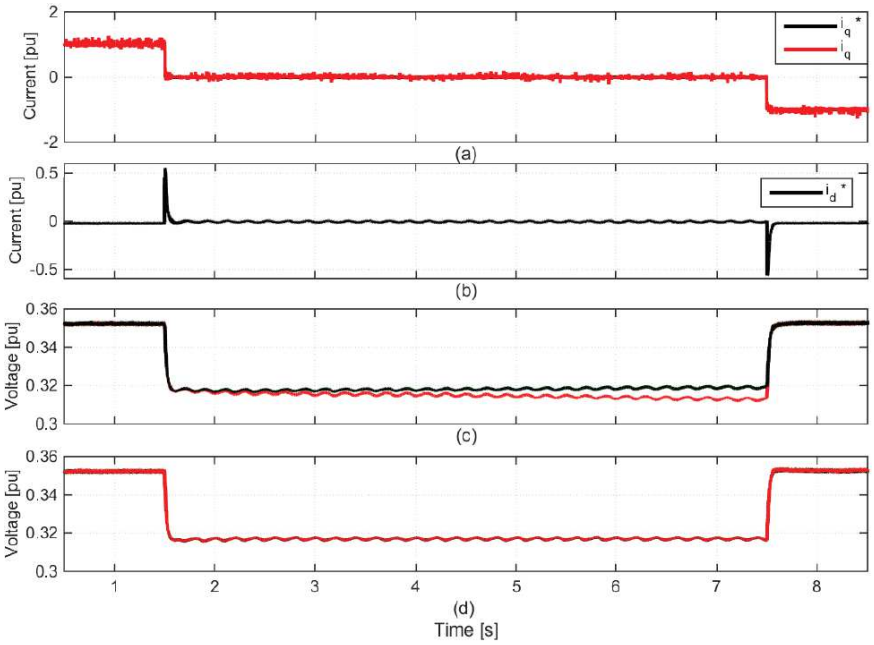

Figure 9 Experimental results. (a) Reference and actual reactive component of the current, (b) Reference active component of current, (c,d) Capacitor voltages in phase *a* by using measured and estimated current in the sorting algorithm, respectively

The individual balancing with dc-link modulation technique is obtained with a very small value of the amplitude of the oscillations in the dc-link voltages. Consequently, the current that flows in the phase legs has very small amplitude and will have negligible impact on the grid voltage. To observe the effect of the dc-link modulation on the grid voltage, the proposed method is experimentally applied to a weak grid set-up as shown in Figure 10. Inductors with $L_g = 40$ mH are connected in series with the ac power supply (see Figure 8) at each phase in order to model the grid impedance at weak grid conditions. $L_g = 40$ mH corresponds to short circuit ratio of 1.6 according with the system parameters reported in Article I.

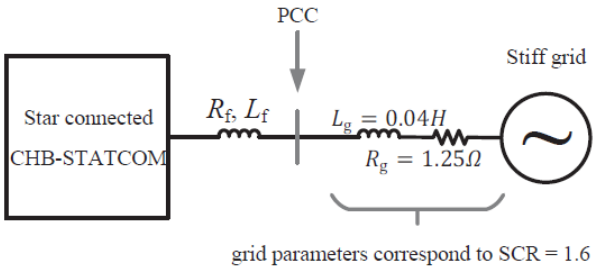

Figure 10 Equivalent circuit diagram of the Y-CHB-STATCOM connected to the weak grid

Figure 11 shows the experimental results of the PCC voltage amplitude and capacitor voltages in phase *a*. The reference reactive current is set to -0.12 pu and then it is changed to zero and 0.12 pu at t=1.5 s and t=7.5 s respectively. Figure 11 (a) shows the grid voltage amplitude, and Figure 11 (b) shows the capacitor voltages in phase *a* with and without the dc-link modulation technique. It can be observed that while the dc-link voltage modulation technique is able to provide appropriate

balancing among the dc-links under the weak grid condition, it has negligible impact on the PCC voltage amplitude.

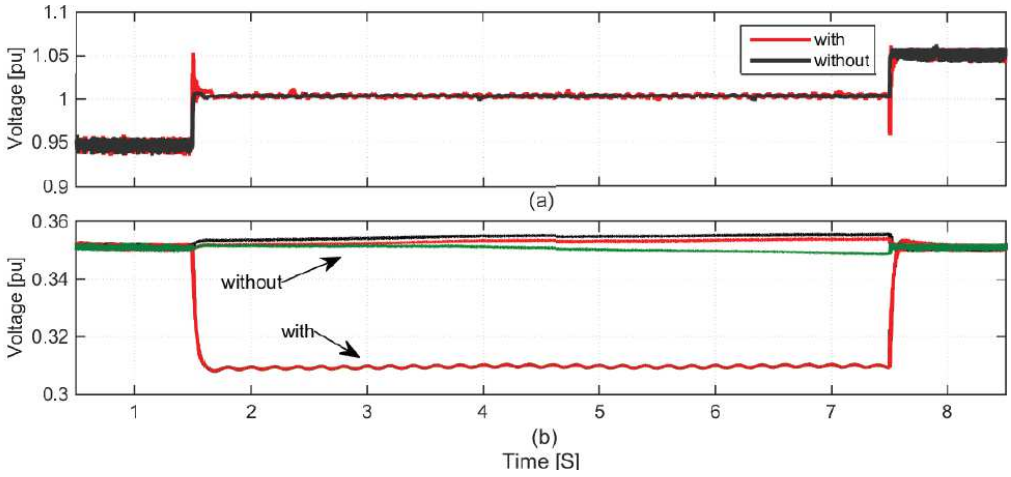

Figure 11 Experimental results with the weak grid, (a) PCC voltage amplitude with and without dc-link voltage modulation technique, (b) dc-link voltages in phase *a* with and without dc-link voltage modulation technique

I.6 Conclusion

A method for individual dc-link voltage balancing for Y-CHB-STATCOM when operated at zero-current mode has been proposed. The investigated method is based on the introduction of a small dc-link voltage modulation that forces a small active power exchange between the converter and the grid. The resulting active current does not impact the grid voltage at the connection point, even in case of weak grids. Since this current is small and comparable to the current ripple and measurement noise, it is suggested to estimate the current for the sorting process. The proposed method is verified both with a down-scaled laboratory set-up and simulation results. The results show the ability of the proposed method in providing an appropriate individual dc-link voltage balancing at zero-current mode. Although the focus has been on the Y-CHB, the proposed method can be applied to any selected MMC topology.

Part II. Investigation of hybrid converter topologies

As mentioned earlier, the Cascaded H-Bridge (CHB), both in star and delta configuration, show a limited operating range under unbalanced conditions, due to the presence of a singularity point and, thereby, the need for a high over-rating under certain circumstances. Focusing on the CHB star, hybrid converters have been proposed as a solution to reduce the needed over-rating due to the singularity. The idea is to use the CHB star together with a Generic Converter (GC) connected to the converter's neutral point, in order to facilitate the energy exchange between the converter phases. At this part, a control algorithm for the hybrid converter is proposed to obtain an optimal utilization of the GC for STATCOM application and

thus, minimizing the effect of the singularity point in the CHB star. The operating range of the hybrid converter is compared with the classical CHB star. The obtained results demonstrate that the operating range of the hybrid converter can be significantly improved, given that the GC is sufficiently large to circulate the needed energy between the converter phase-legs.

II.1 Hybrid converter topology

The investigated hybrid converter topology is illustrated in Figure 12. The system consists of two parts. The CHB star (denoted as "star part" in the figure) and the GC (displayed inside the dashed rectangle), connected to the neutral point of the star part. No specific topology is considered for the GC. However, it is assumed that it can generate any kind of reference voltages and exchange energy among its phases under any kind of unbalanced scenario[1]. Therefore, the GC in Figure 12 is represented by three controllable ac voltage sources. The hybrid converter is connected to the grid via a filter reactor in each phase. The grid is modeled by a three-phase ac source with series reactors, representing the short-circuit impedance at the connection point. The steady-state operating principle is provided in this section using phasor analysis.

Operating principle

From the demanded positive- and negative-sequence current phasors ($\underline{I}^+, \underline{I}^-$)[2], the converter reference voltages in steady-state are calculated as

Equation 9

$$\underline{V}^+ = \underline{E}^+ - (R_\mathrm{f} + j\omega L_\mathrm{f})\underline{I}^+, \qquad \underline{V}^- = \underline{E}^- - (R_\mathrm{f} - j\omega L_\mathrm{f})\underline{I}^-$$

where $\underline{E}^\pm$ are the Point of Common Coupling (PCC) positive- and negative-sequence voltage phasors, R_f, L_f are the filter resistance and inductance and finally ω is the line angular frequency.

[1] This assumption is made in order to allow the theoretical investigation to find the maximum possible improvement with the hybrid converter. The idea is to provide a comprehensive theoretical investigation with a generic converter rather than focusing on one specific GC topology. The reader should observe that the proposed control approach can be adopted to any specific selected topology for the GC.

[2] Phasor quantities are denoted by underlined capital letters, capital letters indicate the amplitude of the phasor and small letters show the instantaneous terms.

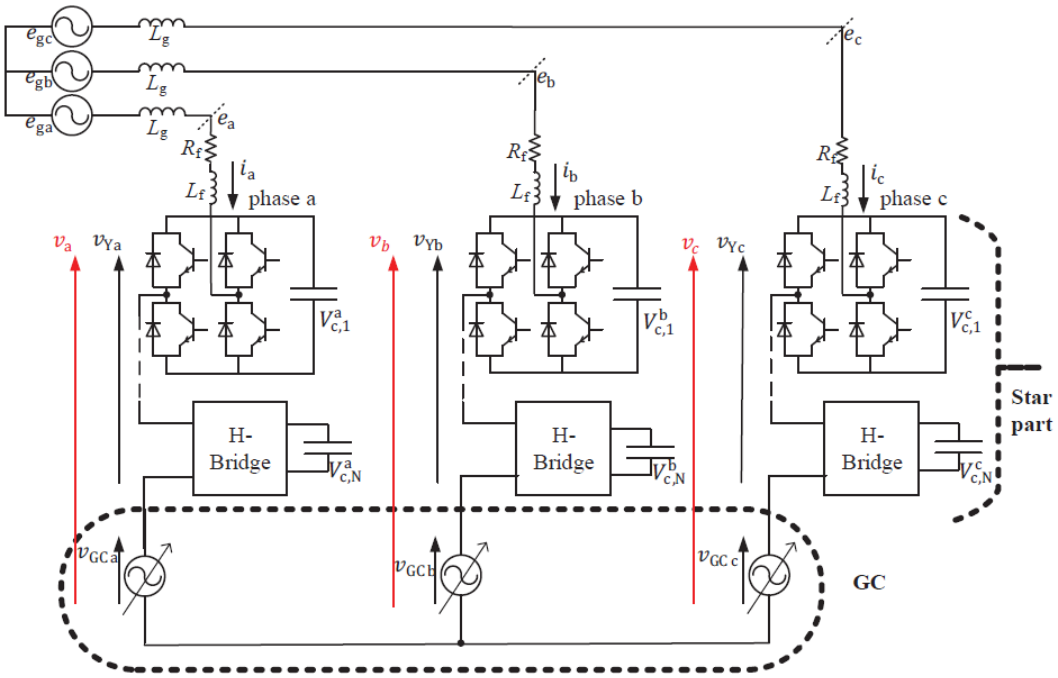

Figure 12 Hybrid converter consisting of CHB star together with GC at the star point

In order to guarantee a stable operation of the hybrid converter, the capacitor voltages at the star part must be kept constant and equal to their reference value. For a lossless converter (100% efficiency), the capacitor voltages can be kept constant by controlling the average active power flowing in each phase of the star part to zero. This is naturally achieved under balanced conditions ($\underline{E}^- = \underline{I}^- = 0$) and when the STATCOM only exchanges reactive power with the grid. Figure 13 (a) illustrates an example of the reference voltage phasor ($\underline{V_a}$) and line current ($\underline{I_a}$) in phase-a under a balanced condition. $\underline{V_a}$ is perpendicular to $\underline{I_a}$, result in zero average active power. For this example, $\underline{V_a}$ is shared between the star part ($\underline{V_{Ya}}$) and the GC ($\underline{V_{GCa}}$) as shown in the figure. $\underline{V_{Ya}}$ and $\underline{V_{GCa}}$ have the same phase angle as $\underline{V_a}$.

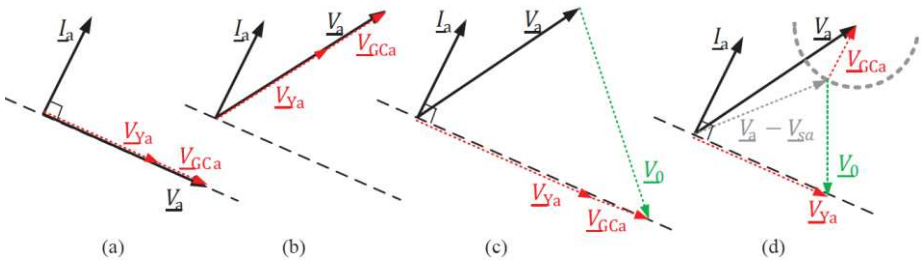

Figure 13 Current and voltage phasors in phase a. (a) balanced condition, (b) unbalanced condition with non-zero average active power on the star part, (c,d) unbalanced condition with two possible voltage sharing to nullify the active power on the star part

For unbalanced conditions, the reference voltage phasor for each phase may not necessarily be perpendicular to its corresponding line current. Figure 13 (b) illustrates $\underline{V_a}$ and $\underline{I_a}$ under a hypothetical unbalanced condition. Sharing $\underline{V_a}$ in the same way as in the balanced case depicted in Figure 13 (a) results in non-zero

average active power in phase-*a* of the star part, which will cause the capacitor voltages in the phase leg to diverge from their reference value.

To nullify the active power during unbalanced conditions, a zero-sequence voltage ($\underline{V}_0$) is normally superimposed to the reference voltage. An example of such scenario is displayed in Figure 13 (c). The resulting reference voltage ($\underline{V}_a$+$\underline{V}_0$) can then be shared between the star part and the GC. Although this can be an approach to utilize the GC, several other possible voltage sharing can also be defined.

To further clarify the concept, Figure 13 (d) shows another voltage sharing example. The arc that is shown with the gray dashed line is part of a circle having radius equal to the voltage rating of the GC. Any voltage phasor inside this circle can be a possible reference voltage for the GC. The resulting $\underline{V}_{Ya}$ with the selected $\underline{V}_{GCa}$ shown in Figure 13 (d) may then be smaller than the previous case. When considering all the three phases and all the possible voltage combinations, there will be a set of three-phase voltage for the GC that leads to a minimum voltage rating for the star part. This is the set of three-phase voltages that must be selected for the GC.

II.2 Proposed algorithm

The basic principle behind the proposed algorithm is to identify all possible voltage phasors for the GC and select the one that results in the minimum voltage rating for the star part. Normally, in STATCOM application the converter cannot exchange active power in steady state due to the lack of an energy storage. This restriction must be considered in the selection of the voltage phasors of the GC. Therefore, solutions resulting in non-zero total active power in the GC are disregarded. The block diagram of the proposed control algorithm is shown in Figure 14 (blue and white blocks) and is described step by step as follows. Note that the positive-sequence grid-voltage phasor is taken as reference here and thus, the quadratic component of the positive-sequence current ($I_q^+ = I^+\sin(\angle\underline{I}^+)$) impacts only the positive-sequence reactive power, while its direct component ($I_d^+ = I^+\cos(\angle\underline{I}^+)$) impacts only the positive-sequence active power. The negative-sequence current ($\underline{I}^-$) is normally perpendicular to the grid negative-sequence voltage in order to avoid negative-sequence active power exchange. Therefore, $\underline{I}^-$ is considered as the negative-sequence reactive current.

Following Figure 14 from top, the maximum voltage rating of the GC ($V_{\mathrm{GC,max}}$) and the demanded reactive currents for each sequence ($\underline{I}^-$ and I_q^+ for the negative- and positive-sequences respectively) are set first. For a lossless converter ($I_d^+ = 0$), $\underline{I}^+$ is calculated next. Having the demanded current phasors, the converter reference voltages are then calculated from Equation 9. Using the symmetrical component basics, the three-phase reference voltage ($\underline{V}_{\mathrm{abc}}$) is calculated next.

At this point the algorithm starts searching between all possible voltage phasors for the GC to find the one that leads to the minimum voltage rating on the star part. For this purpose, a loop is activated where every possible phase angle and amplitude for each phase leg of the GC ($0 \leq \angle\underline{V}_{\mathrm{GC,abc}} < 2\pi$ and $0 \leq V_{\mathrm{GC,abc}} \leq \underline{V}_{\mathrm{GC,max}}$) is

considered. As mentioned earlier, the reference voltages for the GC that result in non-zero total average power must be disregarded. Therefore, the total three-phase power caused by the selected reference voltages for the GC is calculated. If the power is not equal to zero, the considered $\underline{V}_{\mathrm{GC,abc}}$ is disregarded and the loop starts over. Otherwise, the loop continues with calculating the remaining part of the reference voltage ($\underline{V}_{\mathrm{r,abc}}$), which must be synthesized by the star part of the hybrid converter. However, $\underline{V}_{\mathrm{r,abc}}$ may not necessarily result in zero average-power in each phase leg of the star part. Therefore, a zero-sequence voltage must be superposed to $\underline{V}_{\mathrm{r,abc}}$. The required zero-sequence voltage ($\underline{V}_0$) is calculated as:

Equation 10

$$V_0 = \frac{-k_1}{k_3\cos\left(\angle\underline{V}_0\right) + k_4\sin\left(\angle\underline{V}_0\right)}, \qquad \angle\underline{V}_0 = \tan^{-1}\left(\frac{k_2k_3 - k_1k_5}{k_1k_6 - k_2k_4}\right)$$

$$k_1 = \mathrm{Re}\left\{\underline{V}_r^+\underline{I}^{-*} + \underline{V}_r^-\underline{I}^{+*} + \underline{V}_r^0\underline{I}^{-*} + \underline{V}_r^0\underline{I}^{+*}\right\}$$

$$k_2 = \mathrm{Re}\left\{\underline{V}_r^+\underline{I}^{-*}e^{-j4\pi/3} + \underline{V}_r^-\underline{I}^{+*}e^{j4\pi/3} + \underline{V}_r^0\underline{I}^{-*}e^{-j2\pi/3} + \underline{V}_r^0\underline{I}^{+*}e^{j2\pi/3}\right\}$$

$$k_3 = \mathrm{Re}\left\{\underline{I}^- + \underline{I}^+\right\}, \qquad k_4 = \mathrm{Im}\left\{\underline{I}^- + \underline{I}^+\right\}$$

$$k_5 = \mathrm{Re}\left\{\underline{I}^-e^{j2\pi/3} + \underline{I}^+e^{-j2\pi/3}\right\}, \qquad k_6 = \mathrm{Im}\left\{\underline{I}^-e^{j2\pi/3} + \underline{I}^+e^{-j2\pi/3}\right\}$$

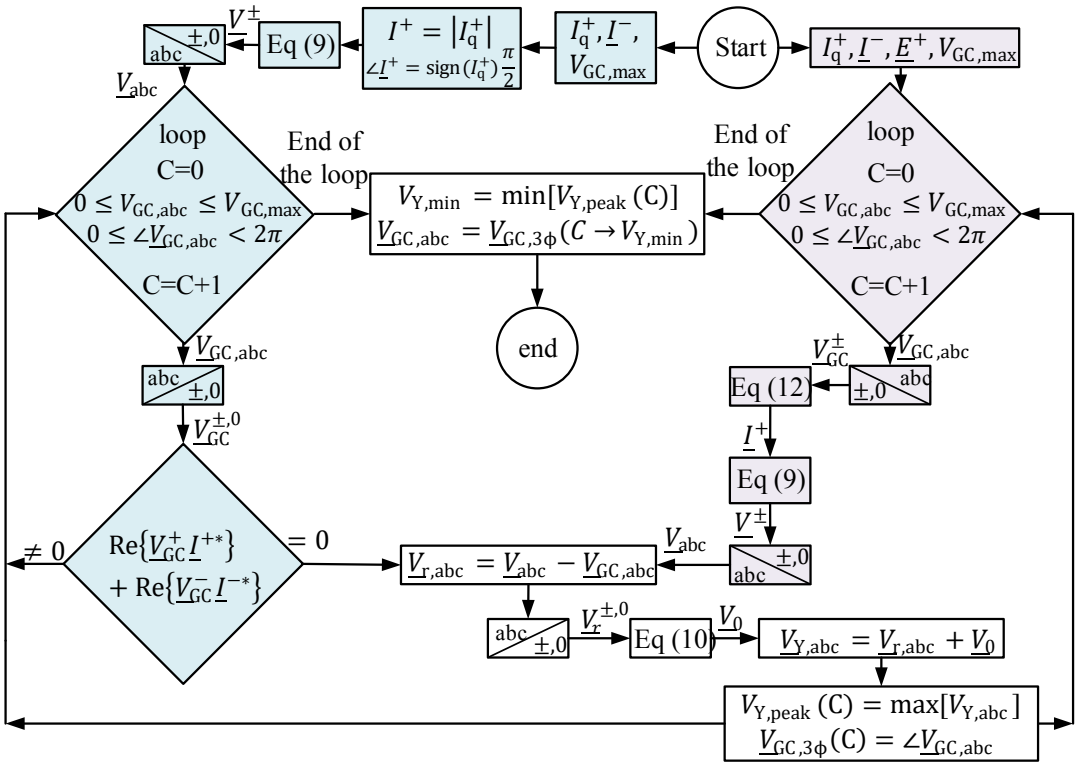

Figure 14 Proposed algorithm for the hybrid converter, blue and white blocks: without energy storage at GC; Gray and white blocks: with energy storage at GC

Thus, the three-phase voltage phasors for the star part ($\underline{V}_{\mathrm{Y,abc}}$) are calculated and the amplitude of the phase leg with the highest peak ($V_{\mathrm{Y,peak}}$) and the selected GC voltage phasors are saved. The loop starts over with a new set of three-phase voltage for the GC. When the loop ends, the minimum value of $V_{\mathrm{Y,peak}}$ among all the saved values shows the lowest possible voltage rating that can be obtained for the star part ($V_{\mathrm{Y,min}}$). The corresponding three-phase reference voltage phasor for the GC are then selected as the optimum reference voltages for the GC.

A special case is when the STATCOM is equipped with a temporary energy storage (for example, super capacitors connected to the dc side of the GC), to facilitate the integration of renewable energy sources into the power systems. In such a case, the available active power can be utilized for balancing purposes and can be used to further minimize the voltage rating of the star part. Note that the resulting active power must be exchanged with the grid to keep the total power on the star part equal to zero. Taking the positive-sequence component of the grid voltage as a reference ($\underline{E}^{+} = E^{+}$) and assuming that the grid voltage is balanced ($\underline{E}^{-} = 0$), the active power flowing in the star part for a given $\underline{I}^{-}$ and I_q^{+} will remain zero if

Equation 11

$$\text{if } I_q^{+} \neq 0 \Rightarrow \mathrm{Re}\{\underline{V}_{GC}^{+}\underline{I}^{+*} + \underline{V}_{GC}^{-}\underline{I}^{-*}\} = E^{+}\mathrm{Re}\{\underline{I}^{+*}\}, \qquad I_q^{+} = I^{+}\sin(\angle\underline{I}^{+})$$

$$\text{if } I_q^{+} \neq 0 \Rightarrow \begin{cases} \angle\underline{I}^{+} = 0, \;\; V_{GC}^{+}I^{+}\cos(\angle\underline{V}_{GC}^{+}) + \mathrm{Re}\{\underline{V}_{GC}^{-}\underline{I}^{-*}\} = E^{+}I^{+} \\ \text{or} \\ \angle\underline{I}^{+} = \pi, \;\; -V_{GC}^{+}I^{+}\cos(\angle\underline{V}_{GC}^{+}) + \mathrm{Re}\{\underline{V}_{GC}^{-}\underline{I}^{-*}\} = -E^{+}I^{+} \end{cases}$$

Thus, $\underline{I}^{+}$is determined by fulfilling Equation 11 as:

Equation 12

$$\text{if } I_q^{+} \neq 0 \Rightarrow \angle\underline{I}^{+} = \tan^{-1}\left[\frac{E^{+}I_q^{+} - V_{GC}^{+}I_q^{+}\cos(\angle\underline{V}_{GC}^{+})}{V_{GC}^{+}I_q^{+}\sin(\angle\underline{V}_{GC}^{+}) + \mathrm{Re}\{\underline{V}_{GC}^{-}\underline{I}^{-*}\}}\right], \qquad I^{+} = \frac{I_q^{+}}{\sin(\angle\underline{I}^{+})}$$

$$\text{if } I_q^{+} = 0 \Rightarrow I^{+} = \left|\frac{\mathrm{Re}\{\underline{V}_{GC}^{-}\underline{I}^{-*}\}}{\underbrace{V_{GC}^{+}\cos(\angle\underline{V}_{GC}^{+}) - E^{+}}_{T}}\right|, \qquad \angle\underline{I}^{+} = \begin{cases} 0 & \text{if } \; T > 0 \\ \pi & \text{if } \; T < 0 \end{cases}$$

The resulting control strategy is shown in Figure 14 (gray and white blocks). The algorithm starts by setting the maximum voltage rating of the GC, demanded $\underline{I}^{-}$ and I_q^{+} and the grid voltage ($\underline{E}^{+}$). Similar to the case explained before, a loop starts

afterwards to evaluate every possible voltage phasor for the GC; as a difference compared with the previous strategy, voltage phasors that result in non-zero total power for the GC are also considered. For each voltage phasor, $\underline{I}^{+}$ is calculated from Equation 12 for power balancing. Thus, the corresponding reference voltages are calculated. The remaining part of the algorithm is the same as for the previous case. At the end of the loop, the minimum value of $\underline{V}_{\mathrm{Y,peak}}$ and the corresponding three-phase reference voltage phasor for the GC are selected.

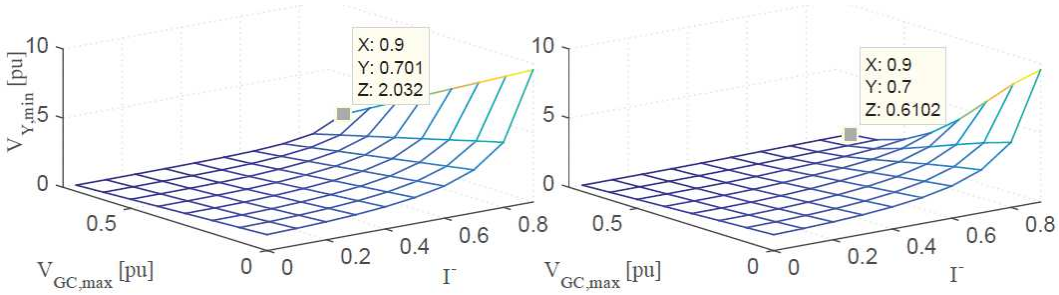

Figure 15 Star part voltage rating versus GC voltage and negative-sequence current, on left without energy storage and on right with energy storage

II.3 Theoretical results

To evaluate the performance of the hybrid converter, several case studies are considered. In all cases, the grid voltage is balanced with amplitude of 1 pu ($\underline{E}^{-} = 0, \underline{E}^{+} = 1$ pu). The positive-sequence reactive current (I_q^{+}) is set to 1 pu capacitive ($I_q^{+} > 0$). This choice is dictated by the fact that capacitive mode imposes higher voltage demands for the converter as compared with the inductive mode. The amplitude of the negative-sequence reactive current (I^{-}) varies from 0 to 0.9 pu. The negative-sequence current angle can be arbitrarily selected in the polar frame, depending on the requirements. However, the negative-sequence current angle that leads to the highest voltage demand for capacitive positive-sequence current is $\angle\underline{I}^{-} = \frac{\pi}{2}$; therefore, this angle is here considered for the negative-sequence current. Finally, a filter reactance and resistance of X_f= 0.15, R_f = 0.015 pu, with ω = 2π 50 rad/s, are considered. It should be highlighted that the case with I^{-}=1 pu (equal positive- and negative-sequence reactive currents) leads to the singularity point, resulting in an infinite zero-sequence voltage demand for the CHB star.

For each of the above mentioned cases, the voltage rating of the GC ($V_{\mathrm{GC,max}}$) varies between 0 pu and 0.7 pu and for each value of $V_{\mathrm{GC,max}}$ the algorithm displayed in Figure 14 calculates the minimum voltage rating that can be obtained for the star part ($V_{\mathrm{Y,min}}$). Figure 15 shows $V_{\mathrm{Y,min}}$ versus $V_{\mathrm{GC,max}}$ and I^{-}. The plot on the left side displays the result without energy storage in the GC, while the plot on the right displays the result with energy storage. Starting with $V_{\mathrm{GC,max}} = 0$ (equivalent to the classical CHB star), it can be observed that an increase in I^{-} leads to an increase in $V_{\mathrm{Y,min}}$; high voltage requirements are obtained when the negative-sequence current

approaches 1 pu (singularity point for the considered operating conditions). Assuming for example that the rated voltage for the star part is 2 pu ($V_{\mathrm{Y,min}} = 2$ pu) and that $V_{\mathrm{GC,max}} = 0$, the operating range is limited to $I^- < 0.6$ pu for the considered case study. With $V_{\mathrm{Y,min}}$ =3 pu the operating range can be extended to $I^- < 0.7$ pu.

Focusing now on the left side figure (no energy storage) and assuming $V_{\mathrm{Y,min}} = 2$ pu and $V_{\mathrm{GC,max}} = 0.7$ pu, the operating range can be extended to I^-<0.9 pu. This means that by a total voltage rating of $V_{\mathrm{tot}} = V_{\mathrm{Y,min}} + V_{\mathrm{GC,max}} = 2.7$ pu, the operating range can be effectively improved as compared with the classical CHB star. Further investigation has shown that with $V_{\mathrm{GC,max}}$=1 pu, any kind of unbalanced condition can be covered. The results on the right side (GC with energy storage) shows additional improvements in the operating range of the hybrid converter, as the same operating range considered in the previous case ($I^- < 0.9$ pu) can now be obtained with $V_{\mathrm{Y,min}}$=2 pu and $V_{\mathrm{GC,max}}$ =0.4 (V_{tot} =2.4 pu).

To further demonstrate the effectiveness of the hybrid converter, Figure 16 (top plots) shows the trend of $V_{\mathrm{Y,min}}$ versus $V_{\mathrm{GC,max}}$ for I^-=[0,0.5,0.9] pu and I_q^+ =1 pu. The bottom plots show the total converter voltage $V_{\mathrm{tot}} = V_{\mathrm{Y,min}} + V_{\mathrm{GC,max}}$ versus $V_{\mathrm{GC,max}}$ for the same cases. Blue and red colors show the results for a system without and with energy storage, respectively. The obtained results show that using GC, not only lower voltage ratings will be required for the star part, but the overall voltage rating of the converter is also reduced as compared with the classical CHB star (equivalent to $V_{\mathrm{GC,max}}$=0). It can also be observed that the GC with energy storage is more effective in reducing the voltage requirement than the GC without energy storage. It should be highlighted that not only the singularity point, but also those operating conditions close to the singularity point, for example I^- =0.9 pu, are practically not feasible to be covered by the CHB star, due to the extremely high voltage requirements. On the other hand, the hybrid converter can effectively extend the operating range of the CHB star with a drastic reduction in the total voltage requirement

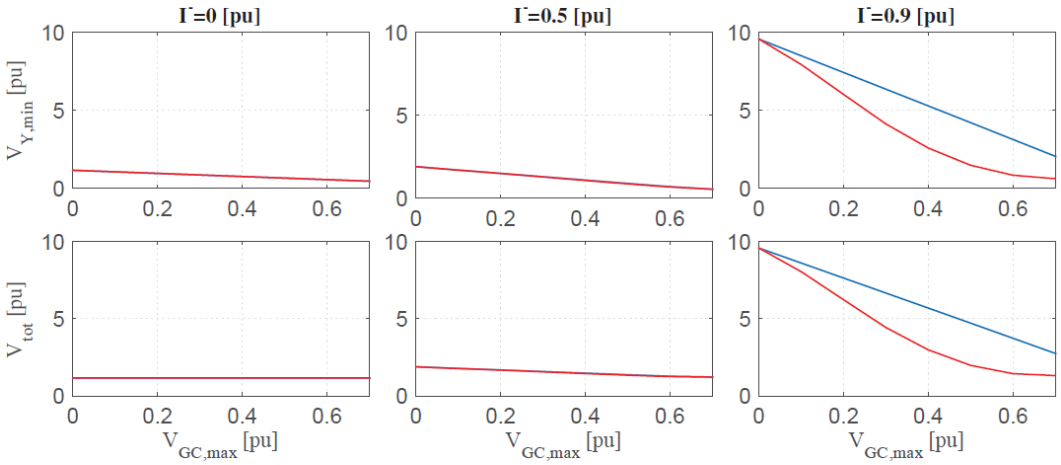

Figure 16 Top plots: star part voltage rating versus GC voltage and bottom plots: total voltage versus GC voltage for $I^ -=0,0.5,0.9$ pu and $I_{\rm q}^{\rm + }=1$ pu, blue: without and red: with energy storage

II.4 Control implementation and simulation results

In this section, the control implementation and simulation results are presented. Figure 17 shows the control block diagram for the hybrid converter in Figure 12. The PCC voltages and line currents are measured and transferred to the *dq*-frame using the transformation angle (θ), which is typically determined by the Phase-Locked Loop (PLL) (not shown in the figure for clarity). The positive- and negative-sequence reference reactive currents $\underline{I}^{-*}, I_q^{+*}$ are set to the desired value, while $I_d^{+*}$is used to control the overall capacitor voltages to the reference value V_c^*. Next, the current controller determines the reference voltage of each phase ($\underline{V}^*_{\mathrm{abc}}$). The reference voltages for the GC ($\underline{V}^*_{\mathrm{GC,abc}}$) are calculated through the algorithm described in Figure 14. The remaining part of the reference voltages ($\underline{V}_{\mathrm{r,abc}}$) are determined by subtracting $\underline{V}^*_{\mathrm{abc}}$ and $\underline{V}^*_{\mathrm{GC,abc}}$. The required zero-sequence voltage needed to nullify the active power in each phase-leg of the star part is then calculated and superposed to the remaining part of the reference voltages, to obtain the reference voltages for the star part ($\underline{V}^*_{\mathrm{Y,abc}}$). The reference voltages in time domain for the star part ($v^*_{\mathrm{Y,abc}}(t)$) and the GC ($v^*_{\mathrm{GC,abc}}$(t)) are finally calculated. The modulators generate the switching pulses for the converters to synthesize the reference voltages for each stage.

The modulation technique for the star part is based on cell sorting approach. At each control cycle, assuming the state of the phase leg is in the charging mode (current direction toward converter and reference voltage and current at each phase have the same sign), the capacitors at each phase are sorted in ascending order. The reference voltage is, thus, modulated using capacitors with the lowest voltage. The same process is used for discharging mode (voltage and current at each phase are in opposite sign). However, at the discharging mode the capacitors with highest voltages are used instead. For The reference voltages for the GC can be directly used for the controllable AC sources.

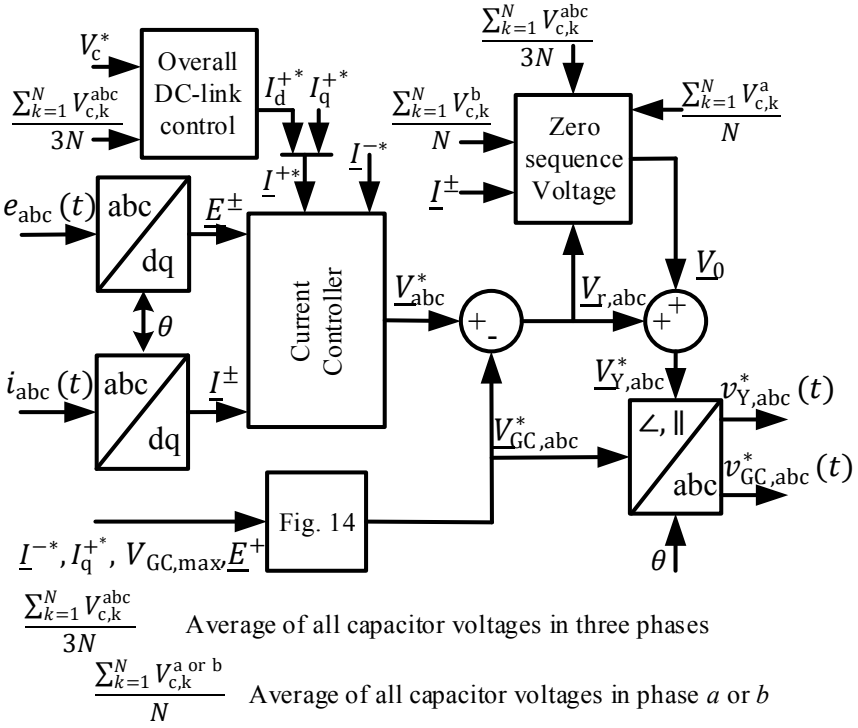

Figure 17 Control block diagram of hybrid converter

II.5 Simulation results

The hybrid converter in Figure 12 is simulated in PSCAD using the control algorithm in Figure 17. The system parameters used for the simulations are reported in Table 3.

Table 3 System parameters in Fig. 1 System parameters in Figure 12

Rated apparent power	S	120 MVA
Grid peak voltage	E_g	27 kV
Grid inductance	L_g	0 H
Filter inductance	L_f	4.3 mH
Filter resistor	R_f	0.136 Ω
DC bus voltage of each cell	V_c^*	27 kV
Cell switching frequency	f_{sw}	2 kHz
Sampling frequency	f_s	6 kHz
Grid frequency	f_0	50 Hz
Number of cells per phase	N	3
Capacitor size	C	4mF

The first simulation is conducted for the hybrid converter without the GC, i.e., the classical CHB star and the obtained results are shown in Figure 18. The per-unit I_q^+ and I^- are shown on the top plots. Per-unit capacitor voltages (V_{cell}), three-phase reference voltage for the star part and GC ($V_{\text{Y,abc}}$ and $V_{\text{GC,abc}}$ respectively) and three-phase line current (i_{abc}) are shown respectively from top after the demanded currents.

The I_q^+ is set to 1 pu for the entire simulation time while I^- is set to zero at t=0 s and then increased in steps of 0.1 pu after each 0.05 s. Three voltage ratings of 2, 2.5 and 3 pu are considered for the CHB star. Starting with the 2 pu voltage limit for the CHB star, it can be observed that by increasing the negative-sequence current, the reference voltages for the CHB star are increased until they hit the limit of 2 pu at t=0.3 s, which corresponds to I^- =0.6 pu. A hard limiter limits the voltage references to avoid over modulation. Consequently, higher negative-sequence current demand will lead to diverging capacitor voltages. With 2.5 and 3 pu voltage ratings for the CHB star, the operating range of the converter is extended up to I^- =0.7 pu. The simulation results are well matched with the obtained theoretical results.

The second performed simulation considers the hybrid converter including the GC with no active-power exchange capability. The same operating conditions as for the previous case study are considered. The maximum voltage rating of the star part (V_{Ymax}) is set to 2 pu. Three voltage ratings for the GC are considered $V_{\text{GC,max}}$ =0.1, 0.4 and 0.7 pu) and the obtained results are shown in Figure 19 (a).

Starting with $V_{\text{Ymax}} = 2$ pu and $V_{\text{GC,max}} = 0.1$ pu and then increase the negative-sequence current, $V_{\text{Y,abc}}$ increases until the limit of 2 pu is reached at t=0.3 s, which corresponds to I^-=0.6 pu. This proves that low-voltage rating for the GC does not allow to extend the operating range as compared with the classical CHB star. However, setting $V_{\text{GC,max}}$ to 0.4 and 0.7 pu allows the hybrid converter to properly operate up to I^-=0.8 pu and I^-=0.9 pu, respectively. Note that, as observed before, the CHB star can operate up to I^-=0.7 pu even with the 3 pu voltage rating. These simulations again validate the obtained theoretical results.

The same case study has been considered when assuming that the CB is equipped with a temporary energy storage and the results are displayed in Figure 19 (b). Note that operation up to I^-=1 pu for $V_{\text{GC,max}}$=0.7 pu can be achieved.

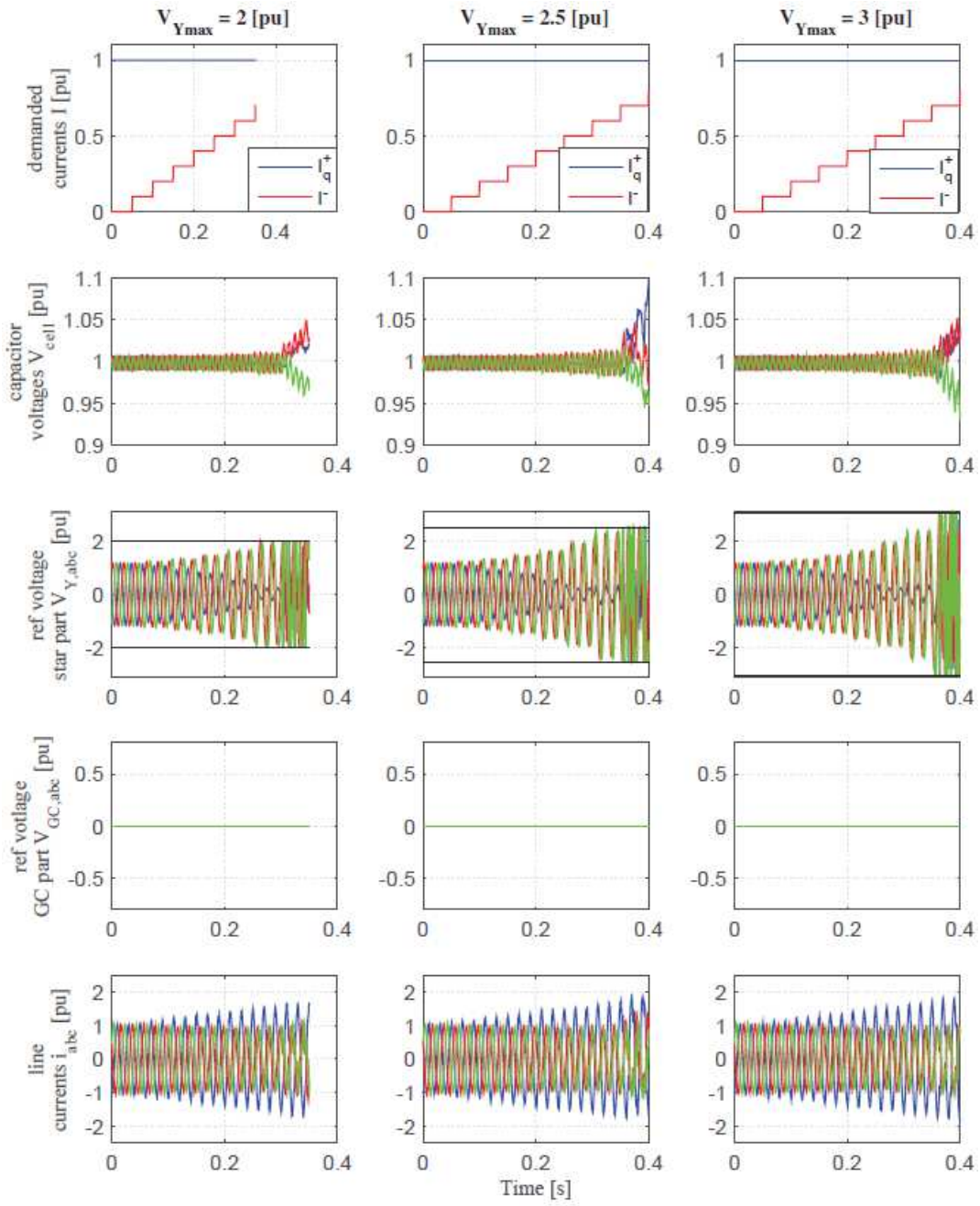

Figure 18 Simulation results of hybrid converter without GC, results from top are: I_q^+ and I^-, capacitor voltages, reference voltage of star, reference voltage of GC and line current

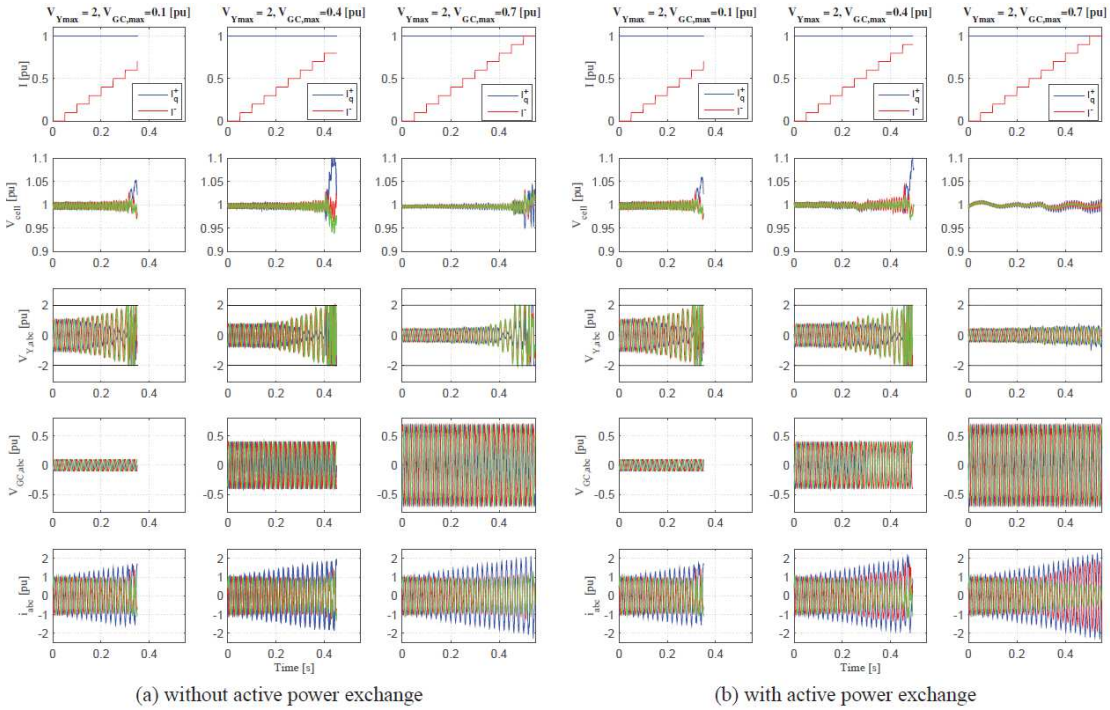

Figure 19 Simulation results of hybrid converter without and with active power exchange capability in (a) and (b) respectively, priority of results are same as in Figure 18

From the obtained results it can be concluded that the use of a hybrid converter effectively allows to extend the operating range of the CHB start when operated under unbalanced conditions. However, it is important to stress that the operating range extension is tightly dependent on the GC's ratings.

II.6 Conclusion

A controller for a hybrid converter for STATCOM applications, based on a Cascaded H-Bridge (CHB) star in series with a generic converter installed at its star point, is proposed and investigated. For a given three-phase reference voltage, the reference voltage for the generic converter is calculated aiming at minimizing the reference voltage of the star part. Thus, the maximum possible operating range for unbalanced currents is achieved. Both cases with and without active power exchange capabilities for the converter are considered in the proposed controller. Theoretical investigation of the hybrid converter using the proposed control approach shows that the operating range of the STATCOM can be significantly extended as compared with the classical CHB star. Temporary active power exchange capability can further extend the operating range. The resulting operating range for the hybrid converter is tightly linked to the ratings of the generic converter, which needs to be sufficiently large to be able to circulate the needed active power between the converter's phase legs. This indicates that, depending on the requirements from the operator in terms of negative-sequence injection capability, the hybrid converter can be a valuable solution to overcome the limitations of the CHB star.

Part III. Double-Y MMC

The double-Y MMC (YYMMC) does not have the limitations associated with the CHB and is, therefore, an attractive alternative topology for STATCOM applications. The YYMMC can be equipped with Half-Bridge (HB) cells or Full-Bridge (FB) cells. Despite the similarity between the two configurations, YYMMC with HB cells is the industrial standard for HVDC applications. Use of FB cells in HVDC has been discussed in the literature, mainly in case of over-head dc transmission due to its functionality during dc line faults. The use of FB cells can be particularly beneficial for STATCOM applications, since it allows any desirable pole-to-pole dc voltage. As a difference compared with HVDC applications, in a STATCOM the dc terminals of the YYMMC are floating and, thus, the pole-to-pole dc voltage can be set to any value. This freedom in the selection of the dc voltage can improve the converter ratings as compared with the YYMMC with half-bridge cells. The classical strategy to balance the capacitor voltages for the YYMMC is based on proper control of the circulating dc currents that flows in the converter's phase-legs. Although effective, this strategy does not lead to an optimal use of the converter, especially in case of unbalanced conditions. In this part of the report, a novel capacitor-voltage balancing strategy for the full-bridge YYMMC STATCOM is proposed and investigated when the system is operated under unbalanced conditions. The proposed strategy, based on zero-sequence voltage injection, manipulates the current distribution between the arms of the YYMMC to avoid the high zero-sequence voltage demand. It is shown that the proposed balancing strategy leads to a reduction of the converter ratings as compared with the classical strategy.

III.1 Capacitor voltage balancing strategies

In this section the issue with the capacitor voltage balancing under unbalanced conditions is described and then the classical and proposed strategies to tackle the issue are presented.

Figure 20 shows the YYMMC connected to a generic ac grid. The cells forming the converter can be either HB or FB cells. From hereafter YYMMC using FB cells will be denoted by YYMMC for simplicity. Note that the YYMMC can be seen as two CHB-Y connected in parallel. The simplified circuit diagram of this topology is illustrated on the right side of Figure 20. In the figure, superscripts $\pm$ represent positive- and negative-sequence components, subscripts u and l represent upper and lower arms respectively, capital letters with over-line represent phasor quantities and finally small letters represent instantaneous quantities.

It is assumed that the YYMMC is loss-less, i.e. for STATCOM operation (only reactive power exchange with the grid) and under balanced conditions the active power exchange in each arm is zero. Therefore, the capacitor voltages will remain constant at their set point. On the other hand, under unbalanced conditions, e.g. when the YYMMC exchanges both positive- and negative-sequence reactive current with the grid, the interaction between the positive- and negative-sequence voltages and currents can cause non-zero and unequal active power distribution

between the converter's phase legs[3]. This causes the capacitor voltages to deviate from their set point.

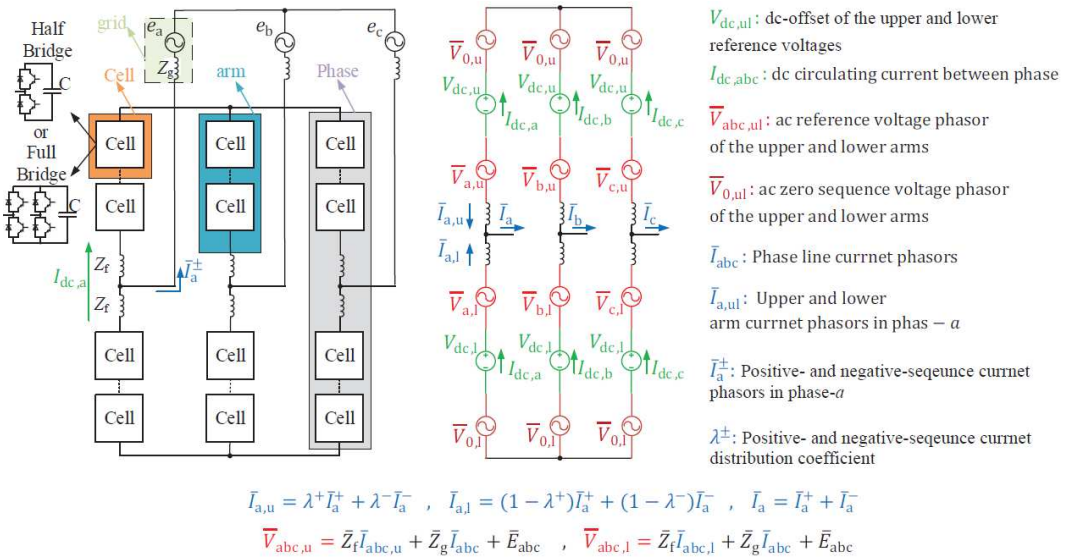

Figure 20 YYMMC and its simplified circuit diagram

To demonstrate this phenomenon, a case when the YYMMC exchanges both positive- and negative-sequence currents with the grid is considered in Figure 21 using PSCAD simulation tool. The line currents are equally distributed between the upper and lower arm of the converter and, therefore, the results are shown only for the upper arm. Figure 21 (a) shows the three-phase upper arm currents ($i_{abc,u}(t)$), (b) shows the three-phase power (calculated as $0.5\mathrm{Re}\left\{\overline{V}_{abc,u}\overline{I}^{*}_{abc,u}\right\}$) and (c) shows the upper arm capacitor voltages in all the three phases. Between 0 and 50 ms, the YYMMC exchanges only positive-sequence current with peak value of 0.55 pu with the grid. During this period, the powers in each phase are zero and capacitor voltages remain at their set point (1 pu). At 50 ms, the YYMMC exchanges 0.1 pu negative-sequence current together with the previous positive-sequence current. Figure 21 (b) shows the resulting unbalanced power that leads to the capacitor voltage deviation, as displayed in Figure 21 (c). To keep the capacitor voltages at their set point, a mechanism to counteract the active power unbalance and force the active power in each phase to zero is therefore required, as described in the following sections.

Classical capacitor-balancing strategy

With this strategy, the ac line current is equally distributed between the upper and lower arms of the YYMMC and the active power unbalance is counteracted by forcing dc currents to flow in the converter legs. Considering the variables definition in Figure 20 this case can be summarized as:

[3] Note that under unbalanced condition the sum of the three-phase power is still zero.

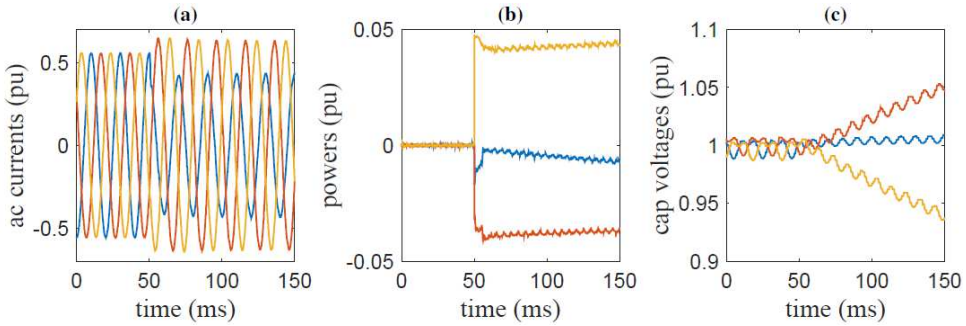

Figure 21Unbalanced active power distribution among the phase-legs of the YYMMC under unbalanced conditions. (a) upper arm three-phase ac-current, (b) upper arm three-phase active power, (c) upper arm capacitor voltages (blue: phase-a, red: phase-b, yellow: phase-c)

Equation 13

$$\lambda^{\pm} = \frac{1}{2}, \bar{I}_{\mathrm{abc,ul}} = \frac{\bar{I}_{\mathrm{abc}}}{2}$$

$$\bar{V}_{\mathrm{abc,u}} = \bar{V}_{\mathrm{abc,l}} = \bar{V}_{\mathrm{abc}}, V_{\mathrm{dc,ul}} = V_{\mathrm{dc}}, V_{0,\mathrm{ul}} = 0$$

$$V_{\mathrm{dc}} I_{\mathrm{dc,abc}} + \mathrm{Re}\left\{\frac{\bar{V}_{\mathrm{abc}} \bar{I}^{*}_{\mathrm{abc}}}{4}\right\} = 0$$

Optimal selection of $\boldsymbol{V_{dc}}$:

For the YYMMC, unlike the YYMMC using HB cells, an infinite number of combinations of $\boldsymbol{V_{dc}}$ and $I_{\mathrm{dc,abc}}$ can be used to force the active power in each arm to zero. Each of these combinations leads to a specific converter rating and, therefore, an algorithm is required to select the optimal $\boldsymbol{V_{dc}}$.

To identify the optimal selection of $\boldsymbol{V_{dc}}$, a case study is here considered. Assume that the converter exchanges $I^{+} = I^{-} = 0.5\angle\frac{\pi}{2}$ pu with a balanced grid of 1 pu voltage ($\bar{E}^{+} = 1$ and $\bar{E}^{-} = 1$pu) and $\bar{Z}_g = 0$. Moreover, the filter reactance X_f is 0.15 pu, while the filter resistance is neglected. In Figure 22 (a), the combinations of $\boldsymbol{V_{dc}}$ and $I_{\boldsymbol{dc},\mathrm{abc}}$ for $0.3 \leq \boldsymbol{V_{dc}} \leq 0.7$ pu that fulfill Equation 13 are displayed. The converter ratings, defined as energy variation ΔW (from hereafter shown with W and called "energy" for simplicity) and semiconductor ratings S, are then calculated for each arm as:

Equation 14

$$w_{\mathrm{abc}}(t) = \int (v_{\mathrm{abc}}(t) + V_{\mathrm{dc}})(i_{\mathrm{abc}}(t)/2 + I_{\mathrm{dc,abc}})dt$$

$$W = \max[\text{peak to peak}\{w_{\mathrm{abc}}(t)\}]$$

$$S = \max[(V_{\mathrm{abc}}(t) + V_{\mathrm{dc}})]\max[I_{\mathrm{abc}}/2 + |I_{\mathrm{dc,abc}}|]$$

where $v_{\mathrm{abc}}(t) = V_{\mathrm{abc}}\cos(\omega t + \angle\bar{V}_{\mathrm{abc}})$ and $i_{\mathrm{abc}}(t) = I_{\mathrm{abc}}\cos(\omega t + \angle\bar{I}_{\mathrm{abc}})$with ω the angular frequency. In Equation 14, the instantaneous energy in each arm

($w_{abc}(t)$) is calculated first. Since the average power in each arm is set to zero, $w_{abc}(t)$ contains only oscillatory terms with a specific peak-to-peak value for each arm. The energy rating W is the maximum peak-to-peak value among the arms. The semiconductor rating S is calculated by multiplying the maximum voltage and current among the arms. The overall converter ratings are calculated by multiplying the arm ratings by 6 (total number of arms in YYMMC). The overall ratings are then divided by the base power for normalization.

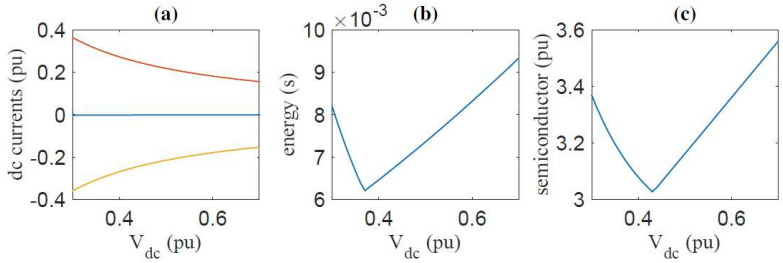

Figure 22 (a) Circulating dc current in each phase $I_{dc,abc}$ and (b,c) normalized energy and semiconductor ratings versus dc voltage V_{dc} for $I^{\pm}$=0.5∠π/2

The normalized energy (expressed in seconds) and semiconductor (in per unit, pu) ratings as a function of V_{dc} are shown in Figure 22 (b) and (c), respectively. From the obtained results, it is possible to observe that a minimum exists both for W and S for certain V_{dc} values.

Note that V_{dc} cannot be arbitrarily changed in an YYMMC with HB cells, as the selection of the dc voltage is dictated by the rated ac voltage.

Proposed capacitor-balancing strategy

In the proposed capacitor-balancing strategy, zero-sequence voltage is utilized to counteract the unbalanced power instead of using dc voltage and dc circulating currents. This strategy can be summarized as

Equation 15

$$V_{\mathrm{dc,ul}} = I_{\mathrm{dc,abc}} = 0, 0 \leq \lambda^{\pm} \leq 1$$

$$\mathrm{Re}\left\{\left(\overline{V}_{0,\mathrm{ul}} + \overline{V}_{\mathrm{abc,ul}}\right)\overline{I}^{*}_{\mathrm{abc,ul}}\right\} = 0$$

Optimal selection of $\lambda^{\pm}$

The basic idea behind the proposed strategy is based on the fact that in a YYMMC different zero-sequence voltages can be applied to the upper and the lower arms of the converter. Thus, the line current can be distributed in any desirable way between the arms, i.e., $0 \leq \lambda^{\pm} \leq 1$ in Figure 20. To determine the optimal values for $\lambda^{\pm}$, and thereby the optimal current distribution between the upper and lower arms, the same case study as in the previous section is here considered. The required zero-sequence voltage for each arm to fulfill Equation 15 are calculated for each selected $\lambda^{\pm}$ as follows:

Equation 16

$$\angle\overline{V}_{0,\mathrm{ul}} = \tan^{-1}\left(\frac{(P_{\mathrm{disb,ul}} - k_{2,\mathrm{ul}})k_{3,\mathrm{ul}} - (P_{\mathrm{disa,ul}} - k_{1,\mathrm{ul}})k_{5,\mathrm{ul}}}{(P_{\mathrm{disb,ul}} - k_{1,\mathrm{ul}})k_{6,\mathrm{ul}} - (P_{\mathrm{disa,ul}} - k_{2,\mathrm{ul}})k_{4,\mathrm{ul}}}\right)$$

$$V_{0,\mathrm{ul}} = \frac{P_{\mathrm{disa,ul}} - k_{1,\mathrm{ul}}}{k_{3,\mathrm{ul}}\cos\left(\angle\overline{V}_{0,\mathrm{ul}}\right) + k_{4,\mathrm{ul}}\sin\left(\angle\overline{V}_{0,\mathrm{ul}}\right)}$$

with

$$k_{1,\mathrm{ul}} = 0.5\mathrm{Re}\left\{\overline{V}^{+}_{\mathrm{a,ul}}\overline{I}^{-*}_{\mathrm{a,ul}} + \overline{V}^{-}_{\mathrm{a,ul}}\overline{I}^{+*}_{\mathrm{a,ul}}\right\}$$

$$k_{2,\mathrm{ul}} = 0.5\mathrm{Re}\left\{\overline{V}^{+}_{\mathrm{b,ul}}\overline{I}^{-*}_{\mathrm{b,ul}} + \overline{V}^{-}_{\mathrm{b,ul}}\overline{I}^{+*}_{\mathrm{b,ul}}\right\}$$

$$k_{3,\mathrm{ul}} = \mathrm{Re}\left\{\overline{I}_{\mathrm{a,ul}}\right\}, k_{4,\mathrm{ul}} = \mathrm{Im}\left\{\overline{I}_{\mathrm{a,ul}}\right\}$$

$$k_{5,\mathrm{ul}} = \mathrm{Re}\left\{\overline{I}_{\mathrm{b,ul}}\right\}, k_{6,\mathrm{ul}} = \mathrm{Im}\left\{\overline{I}_{b,\mathrm{ul}}\right\}$$

where the terms $P_{\mathrm{disa,ul}}$ and $P_{\mathrm{disb,ul}}$ represent any disturbance powers in phase-*a* and -*b*, which are caused by non-idealities in an actual system. Note that in an ideal system the disturbance powers are zero. Thus, for theoretical investigations, $P_{\mathrm{disa,ul}}$ and $P_{\mathrm{disb,ul}}$ are set to zero.

Once the required zero-sequence voltages are available, the arm energy and semiconductor ratings for each selected $\lambda^{\pm}$ are calculated from Equation 17 and the normalized results are shown in Figure 23. Thus, by minimizing the semiconductor or energy ratings the optimal values for $\lambda^{\pm}$ can be determined.

Equation 17

$$w_{\mathrm{abc,ul}}(t) = \int (v_{\mathrm{abc,ul}}(t) + v_{\mathrm{o,ul}}(t))(i_{\mathrm{abc,ul}}(t))dt$$

$$W = \max\left[\text{peak to peak}\left\{w_{\mathrm{abc,ul}}(t)\right\}\right]$$

$$S = \max[|\overline{V}_{\mathrm{abc,ul}} + \overline{V}_{0,\mathrm{ul}}|)]\max[I_{\mathrm{abc,ul}}]$$

where $v_{\mathrm{o,ul}}(t) = V_{0,\mathrm{ul}}\cos\left(\omega t + \angle\overline{V}_{0,\mathrm{ul}}\right)$.

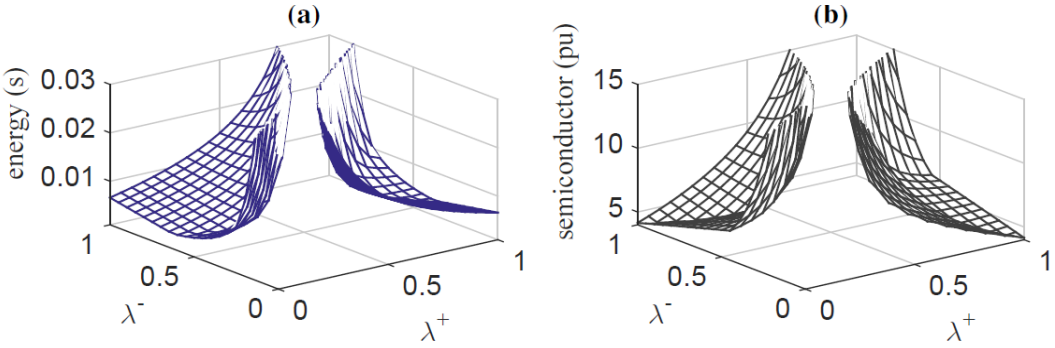

Figure 23 (a) normalized energy, and (b) semiconductor ratings versus $\lambda^{\pm}$ for $I^{\pm}$=0.5∠π/2 with the proposed strategy

As mentioned earlier, the selected case study ($I^+ = I^- = 0.5\angle\frac{\pi}{2}$ pu) results in an infinite zero-sequence voltage demand for the CHB-Y. However, the extra degree of freedom introduced by the YYMMC allows an asymmetric distribution of the positive- and negative-sequence currents between the arms (by proper selection of $\lambda^{\pm}$), thus avoiding the singularity.

Note that this strategy cannot be used with the YYMMC using HB cells, since the dc voltage cannot be arbitrarily changed.

Combined strategy

The active power unbalance can also be counteracted by combining the classical and the proposed capacitor-balancing strategy, as

Equation 18

$$V_{\mathrm{dc,ul}} I_{\mathrm{dc,abc}} + \mathrm{Re}\left\{\frac{(\overline{V}_{\mathrm{0,ul}} + \overline{V}_{\mathrm{abc,ul}})\overline{I}^{*}_{\mathrm{abc,ul}}}{2}\right\} = 0$$

where the zero-sequence voltages are calculated as in Equation 16 with a minor modification in $K_{1,\mathrm{ul}}$ and $K_{2,\mathrm{ul}}$ as:

Equation 19

$$k_{1,\mathrm{ul}} = 0.5\mathrm{Re}\left\{\overline{V}^{+}_{\mathrm{a,ul}}\overline{I}^{-*}_{\mathrm{a,ul}} + \overline{V}^{-}_{\mathrm{a,ul}}\overline{I}^{+*}_{\mathrm{a,ul}}\right\} + V_{\mathrm{dc,ul}} I_{\mathrm{dc,a}}$$

$$k_{2,\mathrm{ul}} = 0.5\mathrm{Re}\left\{\overline{V}^{+}_{\mathrm{b,ul}}\overline{I}^{-*}_{\mathrm{b,ul}} + \overline{V}^{-}_{\mathrm{b,ul}}\overline{I}^{+*}_{\mathrm{b,ul}}\right\} + V_{\mathrm{dc,ul}} I_{\mathrm{dc,b}}$$

Aiming at minimizing either the semiconductor or energy ratings, the dc voltages ($V_{\mathrm{dc,ul}}$), dc currents ($I_{\mathrm{dc,ab}}$)[4] and $\lambda^{\pm}$ can be selected among all the possible solutions. Arm energy and semiconductor ratings are calculated as

Equation 20

$$w_{\mathrm{abc,ul}}(t) = \int (v_{\mathrm{abc,ul}}(t) + v_{\mathrm{o,ul}}(t) + V_{\mathrm{dc,ul}})(i_{\mathrm{abc,ul}}(t) + I_{\mathrm{dc,abc}})dt$$

$$W = \max\left[\text{peak to peak}\left\{w_{\mathrm{abc,ul}}(t)\right\}\right]$$

$$S = \max\left[\left|\overline{V}_{\mathrm{abc,ul}} + \overline{V}_{\mathrm{0,ul}}\right| + \left|V_{\mathrm{dc,ul}}\right|\right]\max\left[I_{\mathrm{abc,ul}} + \left|I_{\mathrm{dc,abc}}\right|\right]$$

As for the previous case, this strategy can only be implemented in YYMMC.

III.2 Comparison between balancing strategies

In this section, the impact of each balancing strategy on converter ratings are compared. The converter's ratings are calculated for $I^{\pm} = 0.5, \angle\overline{I}^{+} = {}^{\pi}/_{2}, {}^{\pi}/_{6} \leq \angle\overline{I}^{-} \leq {}^{\pi}/_{2}$. Note that for the YYMMC using HB cells, the semiconductor rating in

[4] Note that only $I_{\mathrm{dc,ab}}$ are the variable terms. The dc current in phase-*c* is calculated as $I_{\mathrm{dc,c}} = -I_{\mathrm{dc,a}} - I_{\mathrm{dc,b}}$ since the dc currents should only flow between the arms.

Equation 14 must be multiplied by 0.5 since FB cells have twice the semiconductor components compared with the HB cells. The energy rating can be calculated from Equation 14 without any change. The obtained results are shown in Figure 24. In particular, Figure 24 (a) and Figure 24 (b) show the normalized energy and semiconductor ratings when minimizing energy, while Figure 24 (c) and (d) show the same results when minimizing semiconductor rating. It can be observed that in all cases, the YYMMC shows much lower energy ratings as compared to the YYMMC using HB cells at the price of higher semiconductor ratings; this is of course not surprising, as FB cells have double number of components as compared with HB cells.

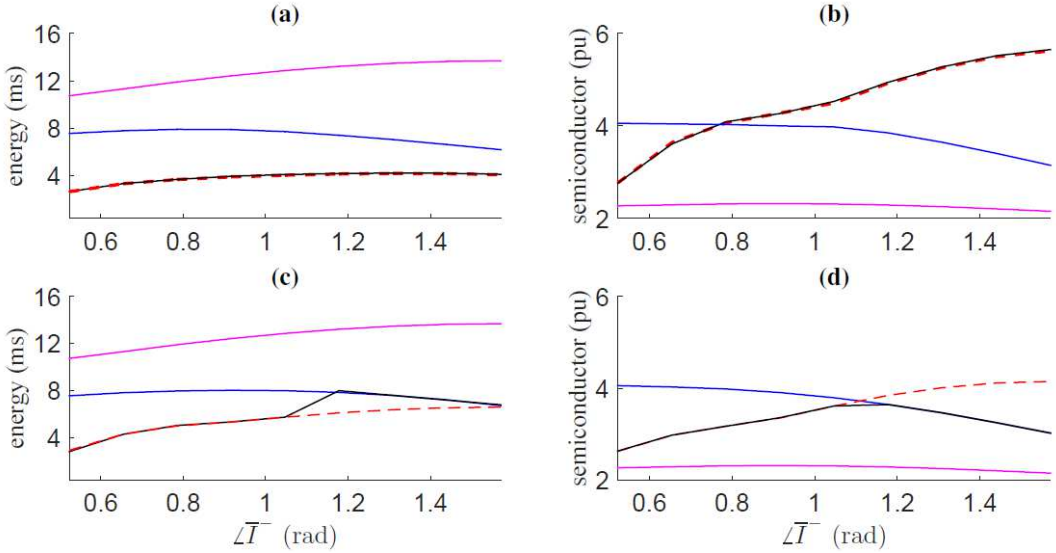

Figure 24 Converter ratings. Magenta(YYMMC using HBs), blue(YYMMC, classical), dashed-red (YYMMC, proposed), Black(YYMMC, combined). (a,b) with *W* minimization; (c,d) with *S* minimization

A quantitative comparison between the considered strategies for the YYMMC together with the case of YYMMC with HB cells is reported in Table 4. Among the three considered balancing strategies, the results for W minimization show that the proposed strategy leads to reduced energy ratings as compared with the classical strategy (similar results are obtained when using the combined strategy). On the other hand, the use of the proposed strategy leads to an increase in the semiconductor ratings. When minimizing S instead, the proposed strategy leads to a 20% reduction in energy with almost no variation in semiconductor rating, indicating the effectiveness of the proposed balancing strategy.

Table 4 Maximum ratings for YYMMC with each strategy

aim	cell type	strategy	$W_{\max}$(ms)	$S_{\max}$(pu)
W minimization	FB	classical	8	4.08
	FB	proposed	4	5.64
	FB	combined	4	5.64
S minimization	FB	classical	8	4.08
	FB	proposed	6.4	4.16
	FB	combined	8	4.24
-	HB	classical	13.6	2.32

III.3 Implementation and experimental verification

The YYMMC STATCOM with the considered balancing strategies is implemented on an experimental set-up. A controller determines the reference voltages, which are then synthesized by a modulator stage. The different parts of the experimental set-up and the obtained results are provided in this section.

Control implementation of classical strategy

The controller output reference voltages for each arm with the classical approach are:

Equation 21

$$v^*_{\mathrm{abc,u}}(t) = v^*_{\mathrm{abc}}(t) + v^*_{\mathrm{dc}} + v'_{\mathrm{dc,abc}}$$

$$v^*_{\mathrm{abc,l}}(t) = v^*_{\mathrm{abc}}(t) - v^*_{\mathrm{dc}} - v'_{\mathrm{dc,abc}}$$

where $v^*_{\mathrm{abc}}(t)$ are the ac reference voltages to enforce the demanded ac currents in the system, v^*_{dc} is the dc voltage reference and $v'_{\mathrm{dc,abc}}$ is to adjust the dc current in each phase leg. Note that $v'_{\mathrm{dc,abc}}$ have not been considered in the theoretical investigation since their values are negligible.

Figure 25 shows the block diagram of the classical strategy. The $v^*_{\mathrm{abc}}(t)$ are calculated by the Current Controller (CC). The CC is implemented in the *dq*-frame for both positive- and negative-sequences using PI-controllers. The line currents and PCC voltages (here $e_{\mathrm{abc}}(t)$ assuming $Z_g = 0$) are measured and transferred to the *dq*-frame using a transformation angle θ, which is calculated using a Phase Locked Loop (PLL). The *dq*-frame is aligned with the grid positive-sequence voltage. Therefore, the direct component of the positive-sequence current reference (i^{+*}_{d}) is used to control the active power and the capacitor voltages in the system. This is done by comparing the average square voltage of all the capacitor voltages ($v^2_{\mathrm{c,avg}}$) with a reference v^{*2}_{c} (where $v^*_{\mathrm{c}}$is the capacitor voltage reference for each cell) and passing the error through a P-controller (P1) to determine the i^{+*}_{d}. Quadratic component of the positive-sequence current reference (i^{+*}_{q}) as well as the negative-sequence current references ($\bar{i}^{-*}$) are determined by the desired positive- and negative-sequence reactive powers. The v^*_{dc} is set to a desired value. Having v^*_{dc}, $v^*_{\mathrm{abc}}(t)$ and the line currents, the required dc current references ($i^*_{\mathrm{dc,abc}}$) to counteract the unbalanced powers in the phase-legs are calculated from Equation 13. The dc currents calculation in Equation 13 does not include the non-idealities such as switching harmonics and disturbances and a small adjustment is required to set the calculated $i^*_{\mathrm{dc,abc}}$ to suitable values. Therefore, the average square voltage of the capacitor voltage in each phase leg ($v^2_{\mathrm{c,avg,abc}}$) is compared with $v^2_{\mathrm{c,avg}}$ and the error is passed through the P-controllers (P2) and then added to the $i^*_{\mathrm{dc,abc}}$ to form the final dc current references. The dc currents are controlled by the P-controller (P3) as shown in Figure 25.

The modulator, based on the cell sorting approach, generates the switching pulses. The basic idea with the cell sorting approach is that at each control cycle, if the state

of the phase leg is in the charging mode (current flows into the positive terminal of the capacitors) then capacitors at each phase are sorted in ascending order. The reference voltage is then modulated using capacitors with the lowest voltage. The same process can be used for the discharging mode. However, at the discharging mode the capacitors with the highest voltages are used instead. With this approach all the capacitor voltages in a phase-leg are equally charged without the need for extra controllers.

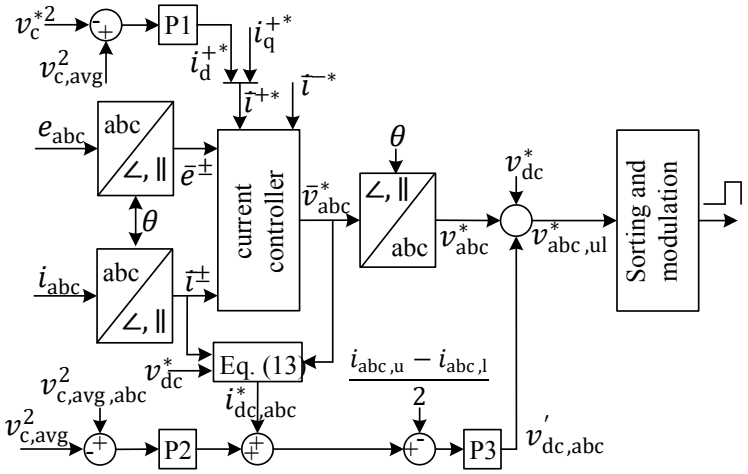

Figure 25 Control block diagram using classical capacitor-balancing strategy

Control implementation of proposed capacitor-balancing strategy

The controller output for each arm with the proposed capacitor-balancing strategy are:

Equation 22

$$v^*_{t,abc,u}(t) = v^*_{abc,u}(t) + v^*_{0,u}(t)$$

$$v^*_{t,abc,l}(t) = v^*_{abc,l}(t) + v^*_{0,l}(t)$$

where $v^*_{abc,u}(t)$ and $v^*_{abc,l}(t)$ are the ac reference voltages for the upper and lower arms to enforce the demanded ac currents in the system and $v^*_{0,u}(t)$ and $v^*_{0,l}(t)$ are the required zero-sequence voltages at each arm for the capacitor voltage balancing purpose.

Figure 26 shows the block diagram of the controller for the upper arm of the converter. A similar controller is also implemented for the lower arm.

Based on the demanded positive- and negative-sequence reactive currents, the upper and lower arm reference reactive currents are determined as described in Section III.1 to either minimize the energy or semiconductor ratings. The total capacitor voltage in each arm is controlled through the corresponding active component of the positive-sequence current reference. As an example, for the upper arm of the converter, displayed in Figure 26, the average square voltage of all the capacitor voltages in the upper arm of the converter ($v^2_{c,avg,u}$) is compared with the

reference (v_c^{*2}) and the error is passed through a P-controller (P4) to determine the $i_{d,u}^{+*}$. The reference currents are then passed through the CC to determine the ac voltages ($\overline{v}_{abc,u}$).

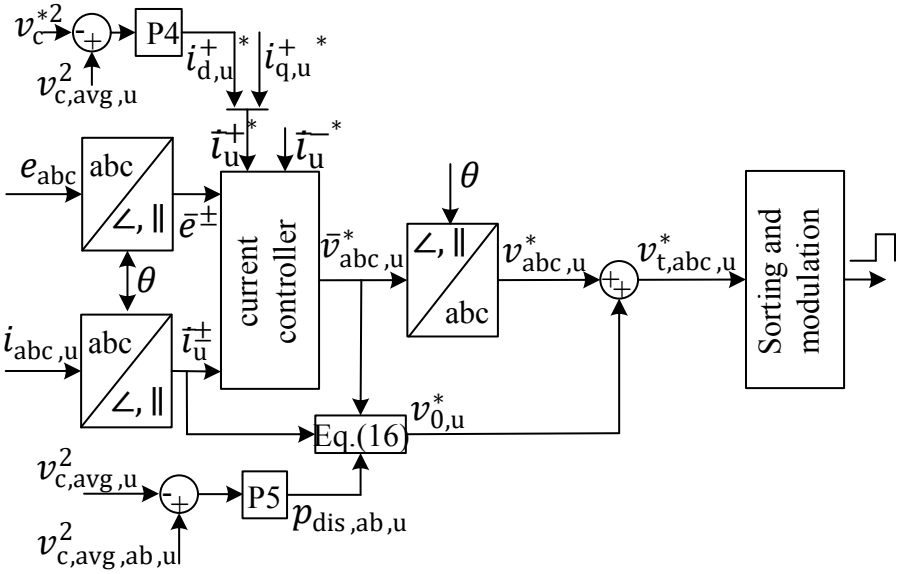

Figure 26 Control block diagram using proposed capacitor-balancing strategy (shown for upper arm only, similar controller is implemented for lower arm as well)

To counteract the unbalanced powers, a zero-sequence voltage is calculated and superposed to the ac voltages. The required zero-sequence voltage is calculated from Equation 16. To take into account the disturbance powers $p_{dis,ab,u}$, the average square voltage of the capacitor voltage in phase-*a* and -*b* of the upper arm ($v_{c,avg,ab,u}^2$) are compared with $v_{c,avg,u}^2$ and the errors are passed through P-controllers (P5).

Once the reference voltage is calculated, the modulator generates the switching pulses with the cell sorting approach, as described earlier.

III.4 Experimental results

Figure 27 shows the implemented experimental set-up. The YYMMC converter is located on the left side of the picture with 6 arms and 2 full-bridge cells per arm. Six filter inductors, one per arm, are located in front of the converter. Computer, dspace controller, and Analog To Digital (A/D) board are located in the middle of the picture. An electronic ac source is used to emulate the connecting the grid, which is located on the right side. The system and control parameters of the experimental set-up are listed in conference article III.

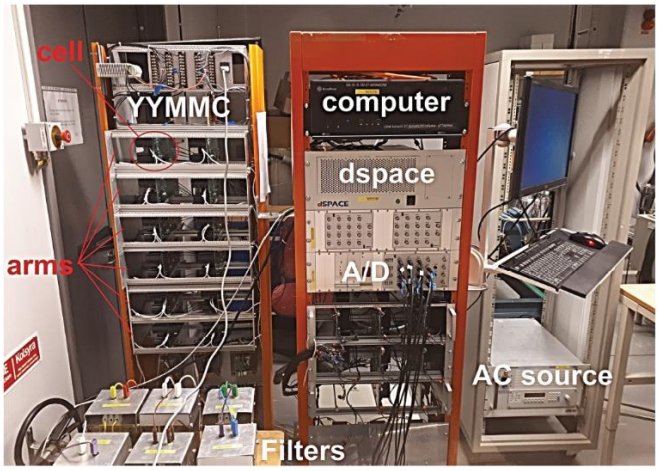

Figure 27 Picture of experimental set-up

Table 5 System and control parameters of the experimental set-up

3-phase rated power	S_b	525 VA
Rated (L-L,RMS) voltage	E^+	60 V
Grid inductance	L_g	0 H
Filter inductance	L_f	17 mH
Filter resistor	R_f	0.5 Ω
Cell capacitor size	C	4 mF
Number of cells per phase	N	2
Grid frequency	f_0	50 Hz
Sampling frequency	f_s	6 kHz
Cell switching frequency	f_{sw}	3 kHz
CC proportional gain, classical strategy	K_{pc}	21.36
CC integral gain, classical strategy	K_{ic}	628.32
CC proportional gain, proposed strategy	K_{pp}	42.72
CC integral gain, proposed strategy	K_{ip}	1256.6
Control gain	P_1	0.013
Control gain	P_2	$0.13/V_{dc}$
Control gain	P_3	2
Control gain	P_4	0.0062
Control gain	P_5	0.13

Experimental results using classical strategy and optimal V_{dc}

According to the results in Figure 24 for the classical strategy, the maximum energy rating among the selected case studies occurs at $\angle\bar{I}^{-} = 0.9$ rad, which is selected as the worst case scenario for the experimental demonstration. Figure 28 (a) shows the capacitor voltage for two different selections of the dc voltage: a non-optimal $v_{\mathrm{dc}}^{*} = 50\,V$, blue curve, and the optimal $v_{\mathrm{dc}}^{*} = 20\,V$, red curve. In the figure, only the capacitor voltage that presents the maximum peak-to-peak variation is depicted for clarity. Analogously, Figure 28 (b) and (c) show the arm current and arm voltage characterized by the maximum peak among all the arms, respectively. Finally, Figure 28 (d) displays the three-phase line current, which is independent from the selected v_{dc}^{*}.

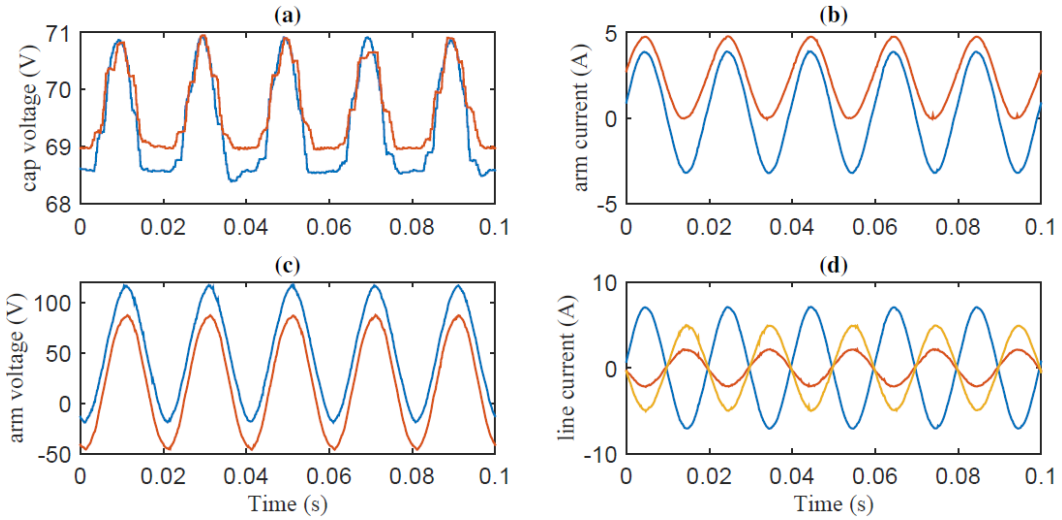

Figure 28 Experimental results of classical strategy with i_{q}^{*}= 0.5 pu (capacitive), $\bar{i}^{-*}$ = 0.5 pu, $\angle\bar{i}^{-*}$ = 0.9 rad, $\bar{e}^{+} = 1$ pu , $\bar{e}^{-} = 0$. (a) capacitor voltage with maximum peak-to-peak voltage variation, (b) and (c) arm current and voltage with maximum peaks and (d) line current. Blue: $v_{dc}^{*} = 50V$, red: $v_{dc}^{*} = 20V$

Figure 28 (a) clearly shows that the optimal selection of V_{dc} results in lower capacitor voltage variation, which corresponds to lower energy rating of the converter. The arm voltage (see Figure 28 (c)) is also reduced, as the dc offset of the reference voltages reduces. The reduction in the peak arm voltage is equal to the reduction of the V_{dc} (30 V). However, the reduction in the V_{dc} leads to an increase in the arm current, as it can be seen from Figure 28 (b), since $I_{dc} \propto {}^{1}/_{V_{dc}}$.

The results obtained can be used to calculate the energy rating of the converter, as

Equation 23

$$W = 0.5CN(V_{\mathrm{c,max}}^{2} - V_{\mathrm{c,min}}^{2})$$

with $V_{\mathrm{c,max}}$ and $V_{\mathrm{c,min}}$ the maximum and minimum value of the capacitor voltage. The arm semiconductor rating is calculated by multiplying the peak values of the arm voltage and current[5].

For the same operating conditions, the dc voltage v_{dc}^{*} is varied between 0.24 pu and 1 pu and the corresponding normalized energy and semiconductor ratings are calculated and depicted in Figure 29. In the figure, the same quantities obtained through the analytical analysis presented in Section III.1 are shown for comparison. It can be observed that beside a small difference between the obtained quantities[6], the trend in the energy and semiconductor ratings is similar for both the theory and the experiment, which clearly indicating that a proper selection of the dc voltage V_{dc} can minimize the energy or semiconductor requirements of the converter.

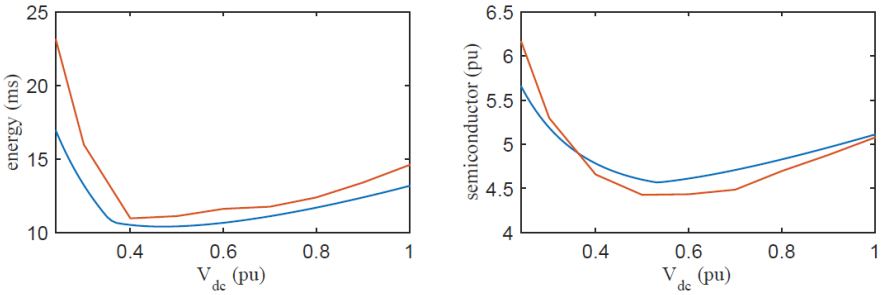

Figure 29 Experimental (in red) and theoretical (in blue) results of normalized energy (on left) and semiconductor ratings (on right) of classical strategy with i_{q}^{*}= 0.5 pu (capacitive), i^{-*} = 0.5 pu, $\angle\bar{i}^{-*}$ = 0.9 rad, $\bar{e}^{+}$ = 1 pu , $\bar{e}^{-}$ = 0 and 0.24≤ v_{dc}^{*} ≤1 pu.

Experimental results using proposed strategy

In order to compare and observe the advantage of the proposed strategy, the same case study as the one presented in the previous section is here considered. Starting with the minimization of the semiconductor rating, the algorithm in Section III.1 calculates the current distribution factors of $\lambda^{\pm}$. The obtained steady-state results with the determined current distribution factors are displayed in Figure 30.

Figure 30 (a) shows the capacitor voltage of the cell with the maximum peak-to-peak voltage variation among all the cells with the proposed strategy (blue), while the red result shows the optimum capacitor voltage obtained previously with the classical strategy (with v_{dc}^{*} =20 V). Figure 30 (b) shows the line current. The line current is similar to the line current in Figure 28 (d) since the same operating condition is considered for both strategies. Figure 30 (c) and (d) show the upper and lower arm voltage and (e) and (f) show the upper and lower arm currents, respectively. Observe that the asymmetrical distribution of the line current leads to asymmetrical upper and lower arm voltage and current.

[5] The overall and normalized ratings can then be calculated by multiplying the results by 6 and dividing by the base power.

[6] Several non-ideal factors such as: forward voltage drop over semiconductors, mismatch between filter inductors, parasitic components, 100 Hz circulating current in the leg, switching dead-time and ac source voltage variations impact the experimental results, which are not considered in the theoretical mode.

Figure 30 (a) clearly shows that the proposed strategy results in lower capacitor voltage variations. The calculated energy rating with the proposed strategy from Equation 23 is 8 ms, which is 26% lower than what is obtained when using the classical strategy. On the other hand, the calculated semiconductor rating when using the proposed strategy is 4.64 pu, which is equal to what has been obtained when using the classical strategy. Thus, for the selected operating condition, the proposed strategy leads to a drastic reduction in the energy rating without compromising the semiconductor rating of the converter as compared with the classical strategy.

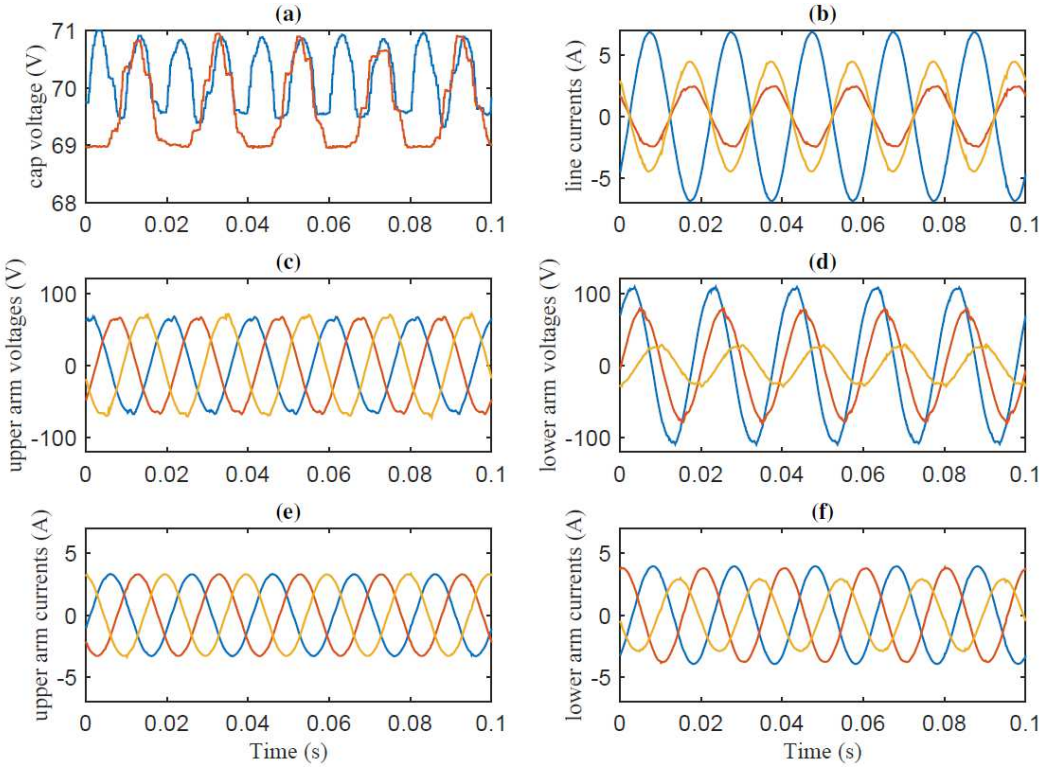

Figure 30 Experimental results of proposed strategy with i_q^*= 0.5 pu (capacitive), $\bar{i}^{-*}$ = 0.5 pu, $\angle\bar{i}^{-*}$ = 0.9 rad, $\bar{e}^{+}$ = 1 pu , $\bar{e}^{-}$ = 0. (a) capacitor voltage with maximum peak-to-peak voltage variation (blue: proposed, red: classical strategy), (b) line current, (c) and (d) upper and lower arm voltage (e) and (f) upper and lower arm current. $\lambda^{+} = 1$ and $\lambda^{-} = 0$ for semiconductor minimization.

The experimental test is repeated with the proposed strategy when aiming at minimizing the energy rating. The optimization algorithm determines the current distribution factors as $\lambda^{+} = 0.97$ and $\lambda^{-} = 0.23$ and the steady-state results are shown in Figure 31. The calculated energy and semiconductor ratings are 6 ms and 4.8 pu, respectively. Therefore, when minimizing the energy, a larger reduction in energy rating can be achieved compared with the classical strategy. However, a slight increase in the semiconductor requirements occurs.

Note that the operating conditions considered for the experimental tests ($\angle\bar{I}^{-} = 0.9$ rad) result in the highest energy rating for the classical strategy (worst case scenario for classical strategy). However, the highest energy rating with the proposed

strategy occurs at $\angle\bar{I}^{-} = \pi/2$ (see Figure 24). Therefore, another experimental test is conducted with the proposed strategy for $\angle\bar{I}^{-} = \pi/2$ for completeness of the investigation. The results of this case study are shown in Figure 32 with (a) showing the capacitor voltages with the highest peak-to-peak voltage variation among all the cell and (b,c) showing the arm voltage and arm current with the highest peak values, respectively (blue: W minimization and yellow: S minimization).

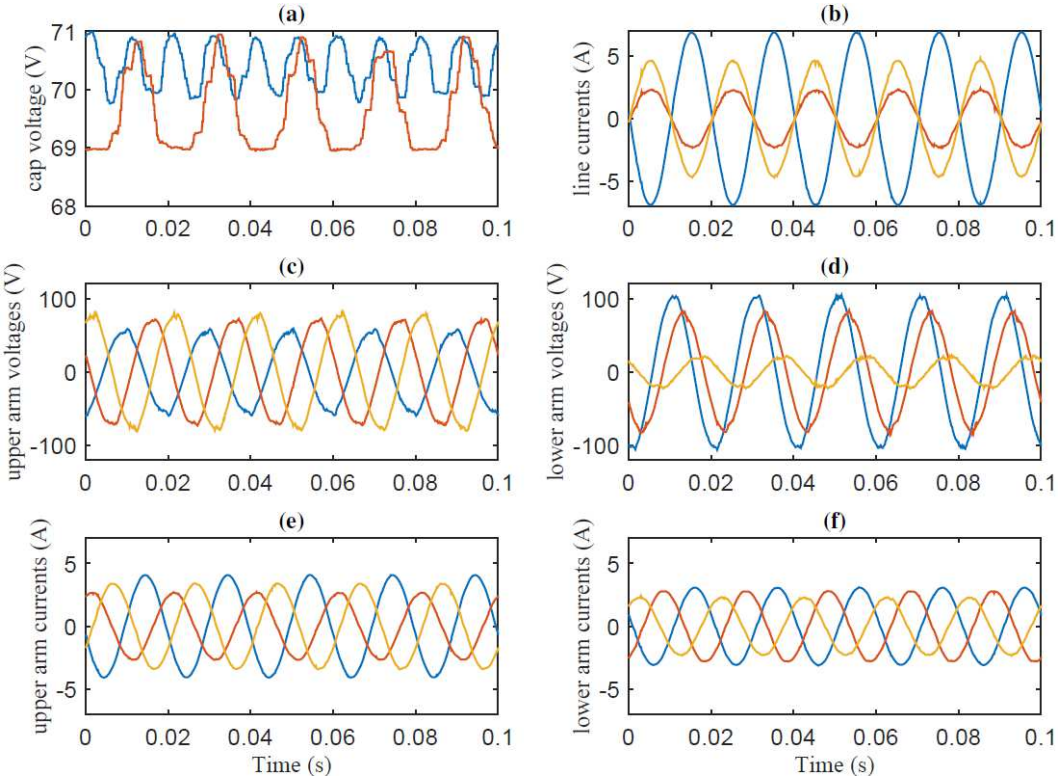

Figure 31 Experimental results of the proposed strategy with similar figure labels and operating condition as in Figure 30 but with energy minimization instead ($\lambda^{+} = 0.97$ and $\lambda^{-} = 0.23$)

From the experimental results and with W minimization, the energy and semiconductor ratings with the proposed strategy are measured as 6 ms and 5.72 pu, respectively. Comparing these results with the results from the worst-case scenario of the classical strategy ($\angle\bar{I}^{-}$ 0.9 rad, W=10.8 ms and S=4.64), the proposed strategy leads to reduced energy ratings but increased semiconductor ratings.

With S minimization instead, the energy and semiconductor ratings are calculated as 8.8 ms and 4.88 pu, respectively. Comparing the worst-case scenarios of both strategies, the proposed strategy leads to 18% reduction in energy with approximately equal semiconductor ratings as compared with the classical one.

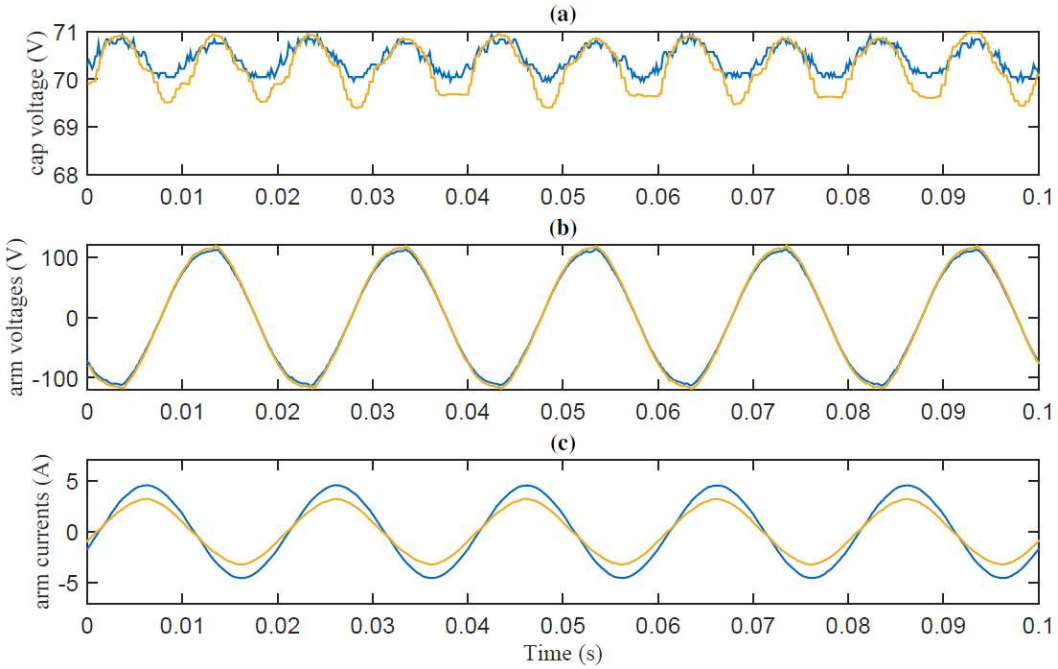

Figure 32 Experimental results of the proposed strategy with $\angle\bar{i}^{-*} = \pi/2$. (a) cap voltages, (b,c) arm voltages and currents, respectively. Blue: W minimization, yellow: S minimization

III.5 Conclusion

In this part of the report, a novel capacitor-voltage balancing strategy for YYMMC STATCOM operated under unbalanced conditions has been presented. The proposed strategy is based on zero-sequence voltage injection and asymmetric distribution of the line current between the converter arms. It has been shown that the use of the proposed balancing strategy results in significant reduction of the converter energy ratings compared to the classical approach without compromising the semiconductor ratings of the device.

Diskussion

Renewable energy sources play, and will play even more in the future, a significant role in the electric power system. In particular, wind and solar installations continue to increase as utilities and power providers are turning to cleaner, more sustainable and abundant sources of energy. However, the future power system will be complex and will require modern tools to guarantee a stable and safe operation. Grid-connected VSCs are important equipment use to enhance the performance of the power system and improve its stability. The most advanced types of VSCs, known as MMCs, are getting more and more attention for the grid applications. Today, CHB configuration, as a well-known subset topology of MMC family, is the industrial standard topology for STATCOM applications and are used for voltage control and reactive power compensation. However, new grid codes and standards for integration of renewable energy sources are demanding more and more negative-sequence reactive power compensation during faults. The investigations that has been done in literature show that the CHB presents severe limitations when the CHB converter is operated under unbalanced conditions; this effectively its limits operating range.

In this project two alternative MMC topologies, know as hybrid converter and double-Y MMC, for STATCOM application have been investigated in detail. Theoretical investigation of the hybrid converter shows that this topology can effectively minimize the impact of the singularity in the CHB; thus, the operating range of the hybrid converter can be significantly extended as compared with the classical CHB. However, the resulting operating range for the hybrid converter is tightly linked to the ratings of the generic converter, which needs to be sufficiently large to be able to circulate the needed active power between the converter's phase legs. This indicates that, depending on the requirements from the system operator in terms of negative-sequence injection capability, the hybrid converter can be a valuable solution to overcome the limitations of the CHB.

The double-Y MMC does not present the limitations associated with the CHB and therefore is an attractive alternative topology for STATCOM applications. However, the conducted theoretical analysis has demonstrated that the classical control approach for this topology does not lead to an optimal utilization of the converter. Therefore, a novel capacitor-voltage balancing strategy for the double-Y MMC STATCOM operated under unbalanced conditions is presented. It is shown that the use of the proposed balancing strategy results in a significant reduction of the converter energy ratings compared to the classical approach without compromising the semiconductor ratings of the device.

According to the obtained results, the double-Y MMC could be the alternative topology for the next generation of STATCOM. In addition to a wide operating range and its ability to exchange negative-sequence power, the presence of the two dc poles in the double-Y MMC facilitates the integration of energy storage, thus enabling temporary active power exchange between the converter and the grid. This feature will increase the number of ancillary services that the converter can provide to the grid, such as inertial support and fast frequency control. The next step in

continuation of this work is to investigate the double-Y MMC in presence of energy storage and to provide an optimized design to minimize the cost of the converter using precise cost functions.

Publikationslista

Journal Articles

I. E. Behrouzian, M. Bongiorno, J. R. Svensson and A. Mohanaveeramani, ” A Proposed Capacitor Voltage-Balancing Strategy for Double-Y STATCOM Operated Under Unbalanced Conditions,” submitted to IEEE Transactions on Industry Applications.

Conference Articles

I. E. Behrouzian and M. Bongiorno,” DC-link voltage modulation for individual capacitor voltage balancing in cascaded H-bridge STATCOM at zero current mode,” in Proc. of European Conference on Power Electronic Applications (EPE), IEEE, 17-21 Sept. 2018.

II. E. Behrouzian, M. Bongiorno and J. R. Svensson,” Operating range extension of cascaded H-bridge star using hybrid converter topology for STATCOM under unbalanced conditions,” in Proc. of European Conference on Power Electronic Applications (EPE), IEEE, 2-6 Sept. 2019.

III. E. Behrouzian, M. Bongiorno, J. R. Svensson and A. Mohanaveeramani,” A Proposed Capacitor Voltage-Balancing Strategy for Double-Y STATCOM Operated Under Unbalanced Conditions,” in Proc. of Energy Conversion Congress and Exposition (ECCE), IEEE, 29 Sept-Oct.3, 2019.

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