A Proposed Capacitor Voltage-Balancing Strategy for Double-Y STATCOM Operated Under Unbalanced Conditions

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***Abstract*—This paper proposes a novel capacitor voltage-balancing strategy for the double-Y MMC STATCOM operated under unbalanced conditions. The proposed method, based on zero-sequence voltage injection, manipulates the current distribution between the converter arms to minimize the converter ratings. The proposed balancing strategy is compared with the classical approach based on controlling the circulating dc currents. For the same unbalanced conditions, the proposed strategy leads to lower energy rating for the converter as compared with the classical one, while the semiconductor ratings remain the same in both strategies. Theoretical findings are verified through simulation results.**

***Index Terms*—modular multilevel converters, double star converter, STATCOM, converter rating, capacitor voltage balancing, unbalanced conditions**

I. Introduction

The static synchronous compensator (STATCOM) is an important member of flexible ac transmission systems (FACTS) family and is utilized for reactive power support and dynamic voltage control. Modular multilevel converters (MMCs), based on series connection of single-phase converter cells, are today the industrial standard for high-power and high-voltage applications, such as STATCOM and HVDC. One challenge with MMCs is the cell-capacitor voltage balancing, especially when the converter is operated under unbalanced system conditions.

In case of STATCOM applications, the most common MMC topology is the Cascaded H-Bridge (CHB) converter [1], where the three converter branches can be connected either in star (CHB-Y) or in delta (CHB-Δ). For these configurations, capacitor-voltage balancing is achieved by controlling either the zero-sequence voltage in case of star [2], [3] or current in case of delta [4], [5]. Literature reports that CHB presents a singularity point that results in very large (up to infinity) demand for the zero-sequence component to keep capacitor-voltage balanced under certain unbalance condition [6], [7]. This represents a limitation for the CHB, especially when considering that new grid codes require negative-sequence current support from the STATCOM [8]. The double-Y MMC (YYMMC) does not have the limitations associated with the CHB and is, therefore, an attractive alternative topology for STATCOM applications [9], [10].

The YYMMC can be equipped with Half-Bridge (HB) cells [11]–[14] or Full-Bridge (FB) cells [15], [16]. Despite the similarity between the two configurations, YYMMC with FB cells is more beneficial for HVDC links with over-head lines due to its functionality during dc line faults [17], [18]. The use of FB cells can be beneficial for STATCOM applications as well, since it allows any desirable pole-to-pole dc voltage. As a difference compared with HVDC applications, in a STATCOM the dc terminals of the YYMMC are floating and, thus, the pole-to-pole dc voltage can be set to any value. This freedom in the selection of the dc voltage can improve the converter ratings as compared with the YYMMC with half-bridge cells [19], [20]. The classical strategy to balance the capacitor voltages for the YYMMC is based on proper control of the circulating dc currents that flows in the converter's phase-legs. Although effective, this strategy does not lead to an optimal use of the converter, especially in case of unbalanced conditions.

The aim of this paper is to propose and investigate a novel capacitor voltage-balancing strategy for the full-bridge YYMMC STATCOM when the system is operated under unbalanced conditions. The proposed strategy, based on zero-sequence voltage injection, manipulates the current distribution between the arms of the YYMMC to avoid the high zero-sequence voltage demand. It is shown that the proposed balancing strategy leads to a reduction of the converter ratings as compared with the classical strategy.

II. Capacitor voltage balancing strategies

In this section the issue with the capacitor voltage balancing under unbalanced conditions is described and then the classical and proposed strategies to tackle the issue are presented.

Fig. 1 shows the YYMMC connected to a generic ac grid. The cells forming the converter can be either HB or FB cells. From hereafter YYMMC using FB cells will be denoted by YYMMC for simplicity. Note that the YYMMC can be seen

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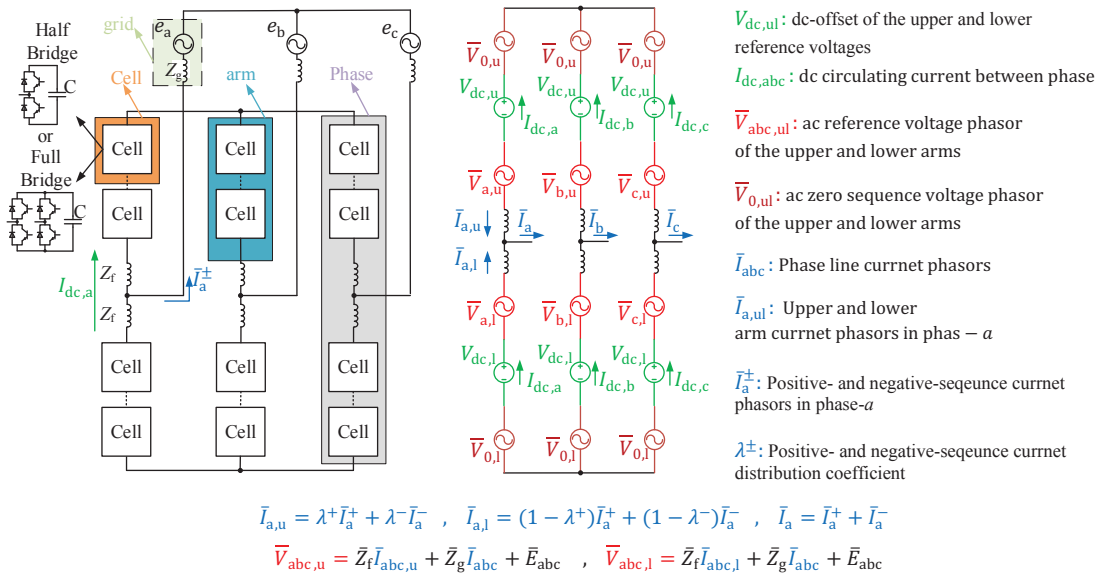

$$\bar{I}_{a,u} = \lambda^{+}\bar{I}_a^{+} + \lambda^{-}\bar{I}_a^{-} \quad , \quad \bar{I}_{a,l} = (1-\lambda^{+})\bar{I}_a^{+} + (1-\lambda^{-})\bar{I}_a^{-} \quad , \quad \bar{I}_a = \bar{I}_a^{+} + \bar{I}_a^{-}$$

$$\overline{V}_{abc,u} = \bar{Z}_f\bar{I}_{abc,u} + \bar{Z}_g\bar{I}_{abc} + \bar{E}_{abc} \quad , \quad \overline{V}_{abc,l} = \bar{Z}_f\bar{I}_{abc,l} + \bar{Z}_g\bar{I}_{abc} + \bar{E}_{abc}$$

Fig. 1. YYMMC and its simplified circuit diagram.

as two CHB-Y connected in parallel. The simplified circuit diagram of this topology is illustrated on the right side of Fig. 1. In the figure, superscripts $\pm$ represent positive- and negative-sequence components, subscripts u and l represent upper and lower arms respectively, capital letters with over-line represent phasor quantities and finally small letters represent instantaneous quantities.

It is assumed that the YYMMC is loss-less, i.e. for STATCOM operation (only reactive power exchange with the grid) and under balanced conditions the active power exchange in each arm is zero. Therefore, the capacitor voltages will remain constant at their set point. On the other hand, under unbalanced conditions, e.g. when the YYMMC exchanges both positive- and negative-sequence reactive current with the grid, the interaction between the positive- and negative-sequence voltages and currents can cause non-zero and unequal active power distribution between the converter's phase legs [1]. This causes the capacitor voltages to deviate from their set point.

To demonstrate this phenomena, a case when the YYMMC exchanges both positive- and negative-sequence currents with the grid is considered in Fig. 2 using PSCAD simulation tool. The line currents are equally distributed between the upper and lower arm of the converter and, therefore, the results are shown only for the upper arm. Fig. 2 (a) shows the three-phase upper arm currents ($i_{abc,u}(t)$), (b) shows the three-phase power (calculated as $0.5\mathrm{Re}\left\{\overline{V}_{abc,u}\overline{I}^{*}_{abc,u}\right\}$) and (c) shows the upper arm capacitor voltages in all the three phases. Between 0 and 50 ms, the YYMMC exchanges only positive-sequence current with peak value of 0.55 pu with the grid. During this period, the powers in each phase are zero and capacitor voltages remain at their set point (1 pu). At 50 ms, the YYMMC exchanges 0.1 pu negative-sequence current together with the previous positive-sequence current. Fig. 2 (b) shows the resulting unbalanced power that leads to the capacitor voltage deviation, as displayed in Fig. 2 (c). To keep the capacitor voltages at their set point, a mechanism to counteract the active power unbalance and force the active power in each phase to zero is therefore required, as described in the following sections.

[1]Note that under unbalanced condition the sum of the three-phase power is still zero.

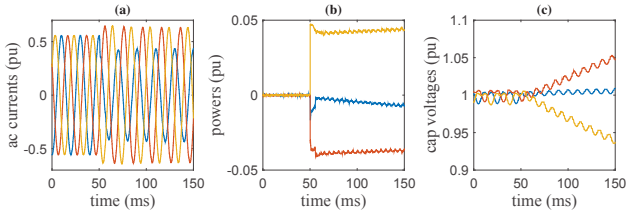

Fig. 2. Unbalanced active power distribution among the phase-legs of the YYMMC under unbalanced conditions. (a) upper arm three-phase ac-current, (b) upper arm three-phase active power, (c) upper arm capacitor voltages (blue:phase-a, red:phase-b, yellow:phase-c).

A. Classical capacitor-balancing strategy

With this strategy, the ac line current is equally distributed between the upper and lower arms of the YYMMC and the active power unbalance is counteracted by forcing dc currents to flow in the converter legs. Considering the variables definition in Fig. 1, this case can be summarized as:

$$\begin{aligned} \lambda^{\pm} &= \frac{1}{2}, \overline{I}_{abc,ul} = \frac{\overline{I}_{abc}}{2} \\ \overline{V}_{abc,u} &= \overline{V}_{abc,l} = \overline{V}_{abc}, V_{dc,ul} = V_{dc}, V_{0,ul} = 0 \\ V_{dc}I_{dc,abc} &+ \mathrm{Re}\left\{\frac{\overline{V}_{abc}\overline{I}^{*}_{abc}}{4}\right\} = 0 \end{aligned} \tag{1}$$

1) Optimal selection of $V_{\rm dc}$: For the YYMMC, unlike the YYMMC using HB cells, infinite combinations of $V_{\rm dc}$ and $I_{\rm dc,abc}$ can be used to force the active power in each arm to zero. Each of these combinations leads to a specific converter rating and, therefore, an algorithm is required to select the optimal $V_{\rm dc}$.

To identify the optimal selection of $V_{\rm dc}$, a case study is here considered. Assume that the converter exchanges $I^+ = I^- = 0.5\angle\pi/2$ pu with a balanced grid of 1 pu voltage ($\overline{E}^+ = 1$ pu, $\overline{E}^- = 0$ pu) and $\overline{Z}_{\rm g} = 0$ pu. Moreover, the filter reactance $X_{\rm f}$ is 0.15 pu, while the filter resistance is neglected. In Fig. 3 (a), the combinations of $V_{\rm dc}$ and $I_{\rm dc,abc}$ for $0.3 \leq V_{\rm dc} \leq 0.7$ pu that fulfill (1) are displayed. The converter ratings, defined as energy variation ΔW (from hereafter shown with W and called energy for simplicity) and semiconductor ratings S, are then calculated for each arm as:

$$\begin{aligned} w_{\rm abc}(t) &= \int \left(v_{\rm abc}(t) + V_{\rm dc}\right)\left(i_{\rm abc}(t)/2 + I_{\rm dc,abc}\right) dt \\ W &= \max\left[\text{peak to peak}\left\{w_{\rm abc}(t)\right\}\right] \\ S &= \max\left[\left(V_{\rm abc} + V_{\rm dc}\right)\right] \max\left[I_{\rm abc}/2 + \left|I_{\rm dc,abc}\right|\right] \end{aligned} \tag{2}$$

where $v_{\rm abc}(t) = V_{\rm abc}\cos\left(\omega t + \angle\overline{V}_{\rm abc}\right)$ and $i_{\rm abc}(t) = I_{\rm abc}\cos\left(\omega t + \angle\overline{I}_{\rm abc}\right)$ with ω the angular frequency. In (2), the instantaneous energy in each arm ($w_{\rm abc}(t)$) is calculated first. Since the average power in each arm is set to zero, $w_{\rm abc}(t)$ contains only oscillatory terms with a specific peak-to-peak value for each arm. The energy rating W is the maximum peak-to-peak value among the arms. The semiconductor rating S is calculated by multiplying the maximum voltage and current among the arms. The overall converter ratings is calculated by multiplying the arm ratings by 6 (total number of arms in YYMMC). The overall ratings is divided by the base power for normalization.

The normalized energy (expressed in seconds) and semiconductor (in per unit pu) ratings as a function of $V_{\rm dc}$ are shown in Fig. 3 (b) and (c), respectively. From the obtained results, it is possible to observe that a minimum exists both for W and S for certain $V_{\rm dc}$ values.

Note that $V_{\rm dc}$ cannot be arbitrarily changed in a YYMMC with HB cells, as the selection of the dc voltage is dictated by the rated ac voltage.

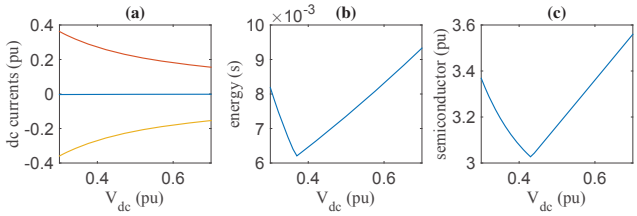

Fig. 3. (a) Circulating dc current in each phase $I_{\rm dc,abc}$ and (b,c) normalized energy and semiconductor ratings versus dc voltage $V_{\rm dc}$ for $I^{\pm} = 0.5\angle\frac{\pi}{2}$.

B. Proposed capacitor-balancing strategy

In the proposed capacitor-balancing strategy, zero-sequence voltage is utilized to counteract the unbalanced power instead of using dc voltage and dc circulating currents. This strategy can be summarized as

$$\begin{aligned} &V_{\rm dc,ul} = I_{\rm dc,abc} = 0\ ,\ 0 \leq \lambda^{\pm} \leq 1 \\ &\text{Re}\left\{(\overline{V}_{0,\rm ul} + \overline{V}_{\rm abc,ul})\overline{I}^{*}_{\rm abc,ul}\right\} = 0 \end{aligned} \tag{3}$$

1) Optimal selection of $\lambda^{\pm}$: The basic idea behind the proposed strategy for YYMMC is that different zero-sequence voltages can be applied to the upper and the lower arm of the converter. Thus, the line current can be distributed in any desirable way between the arms, i.e., $0 \leq \lambda^{\pm} \leq 1$ in Fig. 1. To determine the optimal value for $\lambda^{\pm}$, and thereby the optimal current distribution between the upper and lower arms, the same case study as in the previous section is considered. The required zero-sequence voltage for each arm to fulfill (3) are calculated in the same way as in [7] for each selected $\lambda^{\pm}$. The calculations are summarized as follows:

$$\begin{aligned} \tan\angle\overline{V}_{0,\rm ul} &= \frac{(P_{\rm disb,ul} - K_{2,\rm ul})K_{3,\rm ul} - (P_{\rm disa,ul} - K_{1,\rm ul})K_{5,\rm ul}}{(P_{\rm disb,ul} - K_{1,\rm ul})K_{6,\rm ul} - (P_{\rm disa,ul} - K_{2,\rm ul})K_{4,\rm ul}} \\ V_{0,\rm ul} &= \frac{P_{\rm disa,ul} - K_{1,\rm ul}}{K_{3,\rm ul}\cos(\angle\overline{V}_{0,\rm ul}) + K_{4,\rm ul}\sin(\angle\overline{V}_{0,\rm ul})} \\ K_{1,\rm ul} &= \frac{1}{2}\text{Re}\left[\overline{V}^{+}_{\rm a,ul}\overline{I}^{-*}_{\rm a,ul} + \overline{V}^{-}_{\rm a,ul}\overline{I}^{+*}_{\rm a,ul}\right] \\ K_{2,\rm ul} &= \frac{1}{2}\text{Re}\left[\overline{V}^{+}_{\rm b,ul}\overline{I}^{-*}_{\rm b,ul} + \overline{V}^{-}_{\rm b,ul}\overline{I}^{+*}_{\rm b,ul}\right] \\ K_{3,\rm ul} &= \frac{1}{2}\text{Re}\left[\overline{I}_{\rm a,ul}\right]\ ,\ K_{4,\rm ul} = \frac{1}{2}\text{Im}\left[\overline{I}_{\rm a,ul}\right] \\ K_{5,\rm ul} &= \frac{1}{2}\text{Re}\left[\overline{I}_{\rm b,ul}\right]\ ,\ K_{6,\rm ul} = \frac{1}{2}\text{Im}\left[\overline{I}_{\rm b,ul}\right] \end{aligned} \tag{4}$$

where the terms $P_{\rm disa,ul}$ and $P_{\rm disb,ul}$ represent any disturbance powers in phase a and b, which are caused by non-idealities in an actual system. In an ideal system the disturbance powers are zero. Thus, for theoretical investigations, $P_{\rm disa,ul}$ and $P_{\rm disb,ul}$ are set to zero.

Once the required zero-sequence voltages are available, the arm energy and semiconductor ratings for each selected $\lambda^{\pm}$ are calculated from (5) and the normalized results are shown in Fig. 4. Thus, by minimizing the semiconductor or energy ratings the optimal values for $\lambda^{\pm}$ can be determined.

$$\begin{aligned} w_{\rm abc,ul}(t) &= \int \left(v_{\rm abc,ul}(t) + v_{0,\rm ul}(t)\right)\left(i_{\rm abc,ul}(t)\right) dt \\ W &= \max\left[\text{peak to peak}\left\{w_{\rm abc,ul}(t)\right\}\right] \\ S &= \max\left[\left|\overline{V}_{\rm abc,ul} + \overline{V}_{0,\rm ul}\right|\right] \max\left[I_{\rm abc,ul}\right] \end{aligned} \tag{5}$$

where $v_{0,\rm ul}(t) = V_{0,\rm ul}\cos(\omega t + \angle\overline{V}_{0,\rm ul})$.

Note that the selected case study ($I^+ = I^- = 0.5\angle\pi/2$ pu) results in an infinite zero-sequence voltage demand for the CHB-Y. However, the extra degree of freedom introduced by the YYMMC allows an asymmetric distribution of the positive- and negative-sequence currents between the arms (by proper selection of λ^+ and λ^-), thus avoiding the singularity.

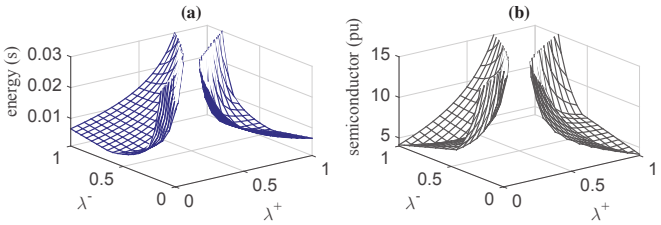

Fig. 4. (a) normalized energy, and (b) semiconductor ratings versus $\lambda^{\pm}$ for $I^{\pm} = 0.5\angle\frac{\pi}{2}$ with the proposed strategy.

Note that this strategy cannot be used with the YYMMC using HB cells, since the dc voltage cannot be arbitrarily changed.

C. Combined strategy

The active power unbalance can also be counteracted by combining the classical and the proposed capacitor-balancing strategy, as

$$V_{\mathrm{dc,ul}} I_{\mathrm{dc,abc}} + \mathrm{Re}\left\{ \frac{\left(\overline{V}_{0,\mathrm{ul}} + \overline{V}_{\mathrm{abc,ul}}\right) \overline{I}^{*}_{\mathrm{abc,ul}}}{2} \right\} = 0 \quad (6)$$

where the zero-sequence voltages are calculated as in (4) with a minor modification in $K_{1,\mathrm{ul}}$ and $K_{2,\mathrm{ul}}$ as:

$$\begin{aligned} K_{1,\mathrm{ul}} &= \frac{1}{2}\mathrm{Re}\left[\overline{V}^{+}_{\mathrm{a,ul}} \overline{I}^{-*}_{\mathrm{a,ul}} + \overline{V}^{-}_{\mathrm{a,ul}} \overline{I}^{+*}_{\mathrm{a,ul}}\right] + V_{\mathrm{dc,ul}} I_{\mathrm{dc,a}} \\ K_{2,\mathrm{ul}} &= \frac{1}{2}\mathrm{Re}\left[\overline{V}^{+}_{\mathrm{b,ul}} \overline{I}^{-*}_{\mathrm{b,ul}} + \overline{V}^{-}_{\mathrm{b,ul}} \overline{I}^{+*}_{\mathrm{b,ul}}\right] + V_{\mathrm{dc,ul}} I_{\mathrm{dc,b}} \end{aligned} \quad (7)$$

Aiming at minimizing either the semiconductor or energy ratings, the dc voltages ($V_{\mathrm{dc,ul}}$), dc currents ($I_{\mathrm{dc,ab}}$)[2] and $\lambda^{\pm}$ can be selected among all the possible solutions. Arm energy and semiconductor ratings are calculated as

$$\begin{aligned} w_{\mathrm{abc,ul}}(t) &= \int \begin{array}{l} \left(v_{\mathrm{abc,ul}}(t) + v_{0,\mathrm{ul}}(t) + V_{\mathrm{dc,ul}}\right) \\ \left(i_{\mathrm{abc,ul}}(t) + I_{\mathrm{dc,abc}}\right) dt \end{array} \\ W &= \max\left[\text{peak to peak}\left\{w_{\mathrm{abc,ul}}(t)\right\}\right] \\ S &= \max\left[\left|\overline{V}_{\mathrm{abc,ul}} + \overline{V}_{0,\mathrm{ul}}\right| + \left|V_{\mathrm{dc,ul}}\right|\right] \max\left[I_{\mathrm{abc,ul}} + \left|I_{\mathrm{dc,abc}}\right|\right] \end{aligned} \quad (8)$$

III. Comparison of Balancing Strategies

In this section, the impact of each balancing strategy on converter ratings are compared. The converter's ratings are calculated for $I^{\pm} = 0.5, \angle\overline{I}^{+} = \pi/2, \pi/6 \leq \angle\overline{I}^{-} \leq \pi/2$. Note that for the YYMMC using HB cells, the semiconductor rating in (2) must be multiplied by 0.5 since FB cells have twice the semiconductor components compared with the HB cells. The energy rating can be calculated from (2) without any change. The obtained results are shown in Fig. 5. In particular, Fig. 5(a) and Fig. 5(b) show the normalized energy and semiconductor ratings when minimizing energy, while Fig. 5 (c) and (d) show the same results when minimizing semiconductor rating. It can be observed that in all cases, the YYMMC shows much lower

[2]Note that only $I_{\mathrm{dc,ab}}$ are the variable terms. The dc current in phase c is calculated as $I_{\mathrm{dc,c}} = -I_{\mathrm{dc,a}} - I_{\mathrm{dc,b}}$ since the dc currents should only flow between the arms.

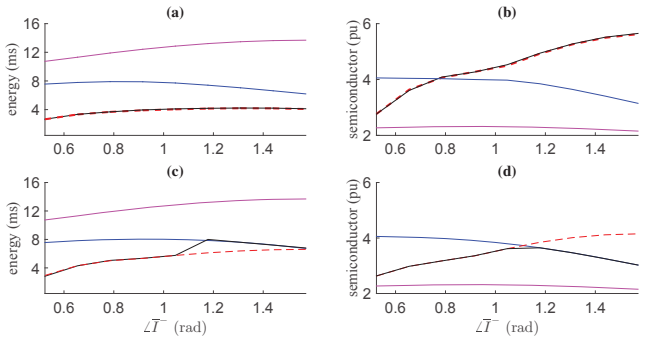

Fig. 5. Converter ratings. Magenta(YYMMC using HBs), blue(YYMMC, classical), dashed-red (YYMMC, proposed), Black(YYMMC, combined). (a,b) with W minimization; (c,d) with S minimization.

TABLE I
MAXIMUM RATINGS FOR YYMMC WITH EACH STRATEGY

aim	cell type	strategy	$W_{\max}$(ms)	$S_{\max}$(pu)
W	FB	classical	8	4.08
minimization	FB	proposed	4	5.64
	FB	combined	4	5.64
S	FB	classical	8	4.08
minimization	FB	proposed	6.4	4.16
	FB	combined	8	4.24
-	HB	classical	13.6	2.32

energy ratings as compared to the YYMMC using HB cells at the price of higher semiconductor ratings; this is of course not surprising, as FB cells have double number of components as compared with HB cells.

A quantitative comparison between the considered strategies for the YYMMC together with the case of YYMMC with HB cells is reported Table I. Among the three considered balancing strategies, the results for W minimization show that the proposed strategy leads to reduced energy ratings as compared with the classical strategy (similar results are obtained when using the combined strategy). On the other hand, the use of the proposed strategy leads to an increase in the semiconductor ratings. When minimizing S instead, the proposed strategy leads to a 20% reduction in energy with almost no variation in semiconductor rating, indicating the effectiveness of the proposed balancing strategy.

IV. Implementation and Simulation Verification

The YYMMC STATCOM with the considered balancing strategies is simulated using PSCAD. A controller determines the reference voltages, which are then synthesized by a modulator stage. The different parts of the simulation model and the obtained results are provided in this section.

A. Control implementation of classical strategy

The controller output (reference voltages) for each arm with the classical approach are:

$$\begin{aligned} v^{*}_{\mathrm{abc,u}}(t) &= v^{*}_{\mathrm{abc}}(t) + v^{*}_{\mathrm{dc}} + v^{'}_{\mathrm{dc,abc}} \\ v^{*}_{\mathrm{abc,l}}(t) &= v^{*}_{\mathrm{abc}}(t) - v^{*}_{\mathrm{dc}} - v^{'}_{\mathrm{dc,abc}} \end{aligned} \quad (9)$$

where $v^*_{\mathrm{abc}}(t)$ are the ac reference voltages to enforce the demanded ac currents in the system, v^*_{dc} is the dc voltage reference and $v'_{\mathrm{dc,abc}}$ is to adjust the dc current in each phase leg. Note that $v'_{\mathrm{dc,abc}}$ were not considered for the theoretical investigation since their values are negligible.

Fig. 6 shows the block diagram of the classical strategy. The $v^*_{\mathrm{abc}}(t)$ are calculated by the Current Controller (CC). The CC is implemented in the $dq-$frame for both positive- and negative-sequences using PI-controllers [21]. The line currents and PCC voltages (here $e_{\mathrm{abc}}(t)$ assuming $Z_{\mathrm{g}} = 0$) are measured and transferred to the $dq-$frame using a transformation angle θ, which is calculated using a Phase Locked Loop (PLL). The $dq-$frame is aligned with the grid positive-sequence voltage. Therefore, the direct component of the positive-sequence current reference ($i_{\mathrm{d}}^{+^*}$) is used to control the active power and the capacitor voltages in the system. This is done by comparing the average square voltage of all the capacitor voltages ($v^2_{\mathrm{c,avg}}$) with a reference v_{c}^{*2} (where v_{c}^* is the capacitor voltage reference for each cell) and passing the error through a P-controller (P1) to determine the $i_{\mathrm{d}}^{+^*}$. Quadratic component of the positive-sequence current reference ($i_{\mathrm{q}}^{+^*}$) as well as the negative-sequence current references ($\bar{i}^{-*}$) are determined by the desired positive- and negative-sequence reactive powers. The v^*_{dc} is set to a desired value. Having v^*_{dc}, $v^*_{\mathrm{abc}}(t)$ and the line currents, the required dc current references ($i^*_{\mathrm{dc,abc}}$) to counteract the unbalanced powers in the phase-legs are calculated from (1). The dc currents calculation in (1) does not include the non-idealities such as switching harmonics and disturbances and a small adjustment is required to set the calculated $i^*_{\mathrm{dc,abc}}$ to suitable values. Therefore, the average square voltage of the capacitor voltage in each phase leg ($v^2_{\mathrm{c,avg,abc}}$) are compared with $v^2_{\mathrm{c,avg}}$ and the errors are passed through the P-controllers (P2) and then added to the $i^*_{\mathrm{dc,abc}}$ to form the final dc current references. The dc currents are controlled by the P-controller (P3) as shown in Fig. 6.

The modulator, based on the cell sorting approach, generates the switching pulses. The basic idea with the cell sorting approach is that at each control cycle, if the state of the phase leg is in the charging mode (current flows into the positive terminal of the capacitors) then capacitors at each phase are sorted in ascending order. The reference voltage is then modulated using capacitors with the lowest voltage. The same process can be used for the discharging mode. However, at the discharging mode the capacitors with the highest voltages are used instead. With this approach all the capacitor voltages in a phase-leg are equally charged without using extra controllers.

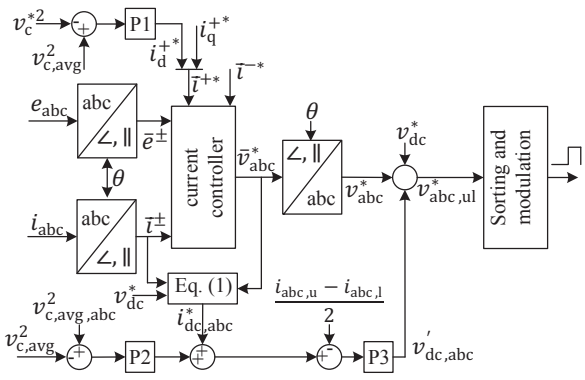

Fig. 6. Control block diagram using classical capacitor-balancing strategy.

B. Control implementation of proposed capacitor-balancing strategy

The controller output for each arm with the proposed capacitor-balancing strategy are:

$$\begin{aligned} v^*_{\mathrm{t,abc,u}}(t) &= v^*_{\mathrm{abc,u}}(t) + v^*_{\mathrm{o,u}}(t) \\ v^*_{\mathrm{t,abc,l}}(t) &= v^*_{\mathrm{abc,l}}(t) + v^*_{\mathrm{o,l}}(t) \end{aligned} \tag{10}$$

where $v^*_{\mathrm{abc,u}}(t)$ and $v^*_{\mathrm{abc,l}}(t)$ are the ac reference voltages for the upper and lower arms to enforce the demanded ac currents in the system and $v^*_{\mathrm{o,u}}(t)$ and $v^*_{\mathrm{o,l}}(t)$ are the required zero-sequence voltages at each arm for the capacitor voltage balancing purpose.

Fig. 7 shows the block diagram of the controller for the upper arm of the converter. A similar controller is also implemented for the lower arm.

Based on the demanded positive- and negative-sequence reactive currents, the upper and lower arm reference reactive currents are determined as described in Section II-B1 to either minimize the energy or semiconductor ratings. The total capacitor voltage in each arm is controlled through the corresponding active component of the positive-sequence current reference. As an example, for the upper arm of the converter, displayed in Fig. 7, the average square voltage of all the capacitor voltages in the upper arm of the converter ($v^2_{\mathrm{c,avg,u}}$) is compared with the reference (v_{c}^{*2}) and the error is passed through a P-controller (P4) to determine the $i_{\mathrm{d,u}}^{+^*}$. The reference currents are then passed through the CC to determine the ac voltages ($\overline{v}_{\mathrm{abc,u}}$).

To counteract the unbalanced powers, a zero-sequence voltage is calculated and superposed to the ac voltages. The required zero-sequence voltage is calculated from (4). To take

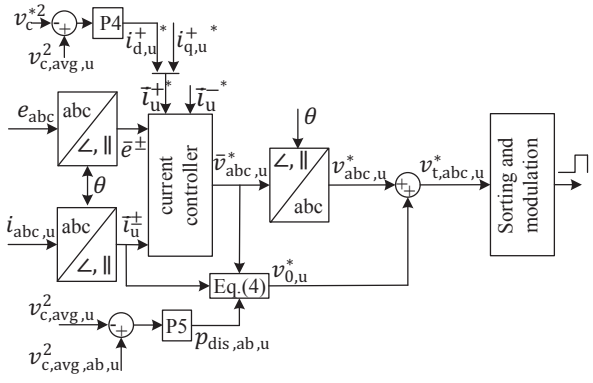

Fig. 7. Control block diagram using proposed capacitor-balancing strategy (shown for upper arm only, similar controller is implemented for lower arm as well).

into account the disturbance powers $p_{\mathrm{dis,ab,u}}$, the average square voltage of the capacitor voltage in phase a and b of the upper arm ($v^2_{\mathrm{c,avg,ab,u}}$) are compared with $v^2_{\mathrm{c,avg,u}}$ and the errors are passed through P-controllers (P5).

Once the reference voltage is calculated, the modulator generates the switching pulses with the cell sorting approach as described earlier.

C. Simulation results

The YYMMC shown in Fig. 1 is simulated in PSCAD. The system and control parameters of the simulation model are listed in Table II. Note that the converter ratings are independent from the number of cells, cell-capacitor voltage and cell-capacitor size; thus, the selection of these values in the simulation model will not impact the verification of the theoretical results. Therefore, also to overcome the limitation in the maximum number of electrical nodes in the simulation program, a low number of high-voltage cells has been selected.

1) Simulation results using classical strategy and optimal selection of V_{dc}: According to the results in Fig. 5 for the classical strategy, the maximum energy rating among the selected case studies occurs at $\angle\overline{I}^{-} = 0.9$ rad, which is selected as the worst case scenario for the simulation demonstration. Fig. 8 (a) shows the simulated capacitor voltage for two different selections of the dc voltage: a non-optimal v^*_{dc}=27 kV, blue curve, and the optimal v^*_{dc}=10.8 kV, red curve. In the figure, only the capacitor voltage that presents the maximum peak-to-peak variation is depicted for clarity. Analogously, Figs. 8 (b) and (c) show the arm current and arm voltage characterized by the maximum peak among all the arms, respectively. Finally, Fig. 8 (d) displays the three-phase line current, which is independent from the selected V_{dc}.

Fig. 8 (a) clearly shows that the optimal selection of V_{dc} results in lower capacitor voltage variation, which corresponds

TABLE II
SYSTEM AND CONTROL PARAMETERS OF THE SIMULATION MODEL

3-phase rated power	Sb	120 MVA
Rated voltage	E^+	33 kV
Grid inductance	L_{g}	0 H
Filter inductance	L_{f}	4.3 mH
Filter resistor	R_{f}	0.14 Ω
Cell capacitor size	C	4 mF
Cell capacitor voltage	V^*_{c}	16 kV
Number of cells per arm	N	4
Grid frequency	f_{o}	50 Hz
Sampling frequency	f_{s}	6 kHz
Cell switching frequency	f_{sw}	1.5 kHz
Simulation time step	t_{sim}	1 μs
CC proportional gain, classical strategy	K_{pc}	5.44
CC integral gain, classical strategy	K_{ic}	176
CC proportional gain, proposed strategy	K_{pp}	10.88
CC integral gain, proposed strategy	K_{ip}	352
Control gain	P_1	0.05
Control gain	P_2	$0.25/V_{\mathrm{dc}}$
Control gain	P_3	20
Control gain	P_4	0.025
Control gain	P_5	0.25

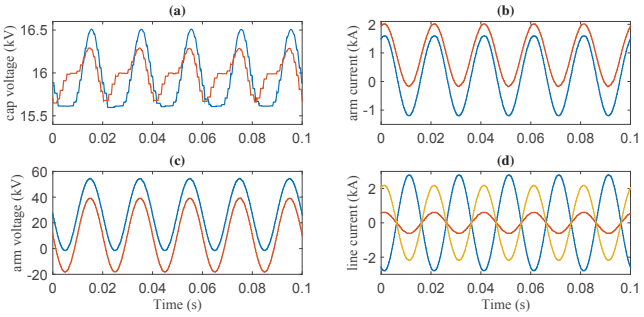

Fig. 8. Simulation results of classical strategy with $i^{+*}_{\mathrm{q}} = 0.5$pu (capacitive),$i^{-*} = 0.5$pu, $\angle\overline{i}^{-*} = 0.9$rad,$\overline{e}^{+} = 1$pu,$\overline{e}^{-} = 0$pu. (a) capacitor voltage with maximum peak-to-peak voltage variation, (b) and (c) arm current and voltage with maximum peaks and (d) line current. Blue: v^{+*}_{dc}=27 kV, red: v^{+*}_{dc}=10.8 kV.

to lower energy rating of the converter. The arm voltage (see Fig. 8 (c)) is also reduced, as the dc offset of the reference voltages reduces. The reduction in the peak arm voltage is equal to the reduction of the V_{dc} (16.2 kV). However, the reduction in the V_{dc} leads to an increase in the arm current, as it can be seen from Fig. 8 (b), since $I_{\mathrm{dc}} \propto 1/V_{\mathrm{dc}}$.

The results obtained can be used to calculate the energy and semiconductor rating of the converter, as

$$W = 0.5CN(V^2_{\mathrm{c,max}} - V^2_{\mathrm{c,max}}) \tag{11}$$

with $V_{\mathrm{c,max}}$ and $V_{\mathrm{c,min}}$ the maximum and minimum value of the capacitor voltage. The arm semiconductor rating is calculated by multiplying the peak values of the arm voltage and current [3].

For the same operating conditions, the dc voltage v^*_{dc} is varied between 0.24 pu and 1 pu and the corresponding normalized energy and semiconductor ratings are calculated and depicted in Fig. 9. In the figure, the same quantities obtained through the analytical analysis presented in Section II-A1 are shown for comparison. As it can be seen from the figure, very good agreement between the simulation and the analytical model is obtained, clearly indicating that a proper selection of the dc voltage V_{dc} can minimize the energy or semiconductor requirements of the converter.

2) Simulation results using proposed strategy: In order to compare and observe the advantage of the proposed strategy, the same case study as the one presented in the previous section is here considered. Starting with the minimization of the semiconductor rating, the algorithm in Section II-B1 calculates the current distribution factors of $\lambda^+ = 0.9$ and $\lambda^- = 0.1$. The obtained steady-state results with the determined current distribution factors are displayed in Fig. 10.

Fig. 10 (a) shows the capacitor voltage of the cell with the maximum peak-to-peak voltage variation among all the cells with the proposed strategy (blue), while the red result shows the optimum capacitor voltage obtained previously with the

[3]The overall and normalized ratings can then be calculated by multiplying the results by 6 and dividing by the base power.

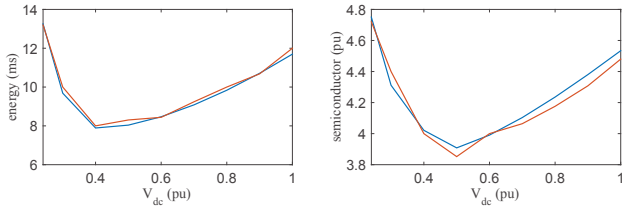

Fig. 9. Simulation (in red) and theoretical (in blue) results of normalized energy (on left) and semiconductor ratings (on right) of classical strategy with $i_{\mathrm{q}}^{+*} = 0.5\mathrm{pu}$ (capacitive),$i^{-*} = 0.5\mathrm{pu}, \angle\overline{i}^{-*} = 0.9\mathrm{rad}, \overline{e}^{+} = 1\mathrm{pu}, \overline{e}^{-} = 0\mathrm{pu}$ and $0.24 \leq v_{\mathrm{dc}}^{*} \leq 1$ pu.

classical strategy (with v_{dc}^{*}=10.8 kV). Fig. 10 (b) shows the line current. The line current is similar to the line current in Fig. 8 (d) since the same operating condition is considered for both strategies. Figs. 10 (c) and (d) show the upper and lower arm voltage and (e) and (f) show the upper and lower arm currents, respectively. Observe that the asymmetrical distribution of the line current leads to asymmetrical upper and lower arm voltage and current.

Fig. 10 (a) clearly shows that the proposed strategy results in lower capacitor voltage variations. The calculated energy rating with the proposed strategy from (11) is 5.2 ms, which is 35% lower than what is obtained when using the classical strategy. On the other hand, the calculated semiconductor rating when using the proposed strategy is 3.4 pu, which is equal to what has been obtained when using the classical strategy. Thus, for the selected operating condition, the proposed strategy leads to a drastic reduction in the energy rating with equal semiconductor rating as compared with the classical strategy.

The simulation is repeated with the proposed strategy when aiming at minimizing the energy rating. The optimization algorithm determines the current distribution factors as $\lambda^{+} = 0.95$ and $\lambda^{-} = 0.3$ and the steady-state results are shown in Fig. 11. The calculated energy and semiconductor ratings are 4 ms and 4.2 pu, respectively. Therefore, When minimizing the energy, a larger reduction in energy rating can be achieved compared with the classical strategy. However, a slight increase in the semiconductor occurs.

Note that the operating conditions considered for the simulation ($\angle\overline{I}^{-} = 0.9$ rad) result in the highest energy rating for the classical strategy (worst case scenario for classical strategy). However, the highest energy rating with the proposed strategy occurs at $\angle\overline{I}^{-} = \pi/2$ (see Fig. 5). Therefore, another simulation is conducted with the proposed strategy for $\angle\overline{I}^{-} = \pi/2$ for completeness of the investigation. The results of this case study are shown in Fig. 12 with (a) showing the capacitor voltages with the highest peak-to-peak voltage variation among all the cell and (b,c) showing the arm voltage and arm current with the highest peak values, respectively (blue: W minimization and yellow: S minimization).

From the simulation results and with W minimization, the energy and semiconductor ratings with the proposed strategy are measured as 4.4 ms and 5.72 pu, respectively. Comparing these results with the results from the worst case scenario of the classical strategy ($\angle\overline{I}^{-} = 0.9$ rad, W=8 ms and S=4), the proposed strategy leads to reduced energy ratings but increased semiconductor ratings.

With S minimization instead, the energy and semiconductor ratings are calculated as 6.4 ms and 4.16 pu, respectively. Comparing the worst case scenarios of both strategies, the proposed strategy leads to 20% reduction in energy with approximately equal semiconductor ratings as compared with the classical one.

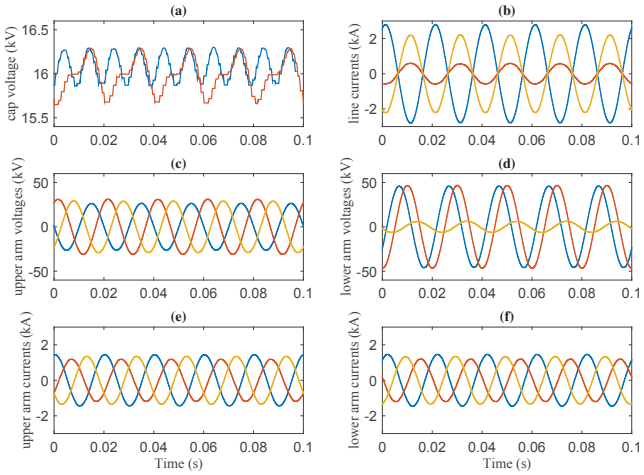

Fig. 10. Simulation results of proposed strategy with $i_{\mathrm{q}}^{+*} = 0.5\mathrm{pu}$ (capacitive),$i^{-*} = 0.5\mathrm{pu}, \angle\overline{i}^{-*} = 0.9\mathrm{rad}, \overline{e}^{+} = 1\mathrm{pu}, \overline{e}^{-} = 0\mathrm{pu}$. (a) capacitor voltage with maximum peak-to-peak voltage variation (blue: proposed, red: classical strategy), (b) line current, (c) and (d) upper and lower arm voltage (e) and (f) upper and lower arm current. $\lambda^{+} = 0.9$ and $\lambda^{-} = 0.1$ for semiconductor minimization.

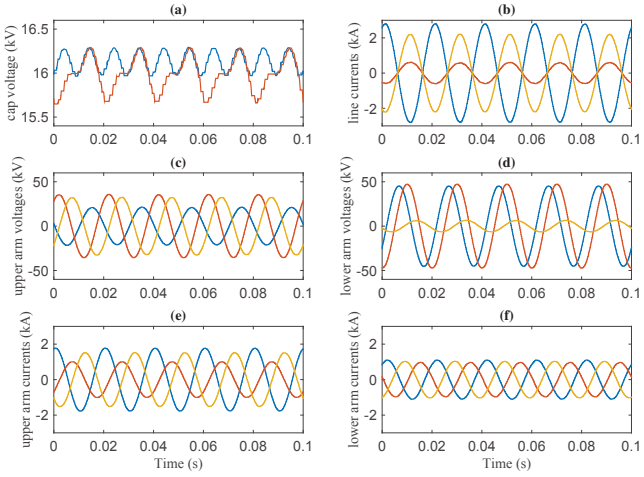

Fig. 11. Simulation results of the proposed strategy with similar figure labels and operating condition as in Fig. 10 but with energy minimization instead ($\lambda^{+} = 0.95$ and $\lambda^{-} = 0.3$).

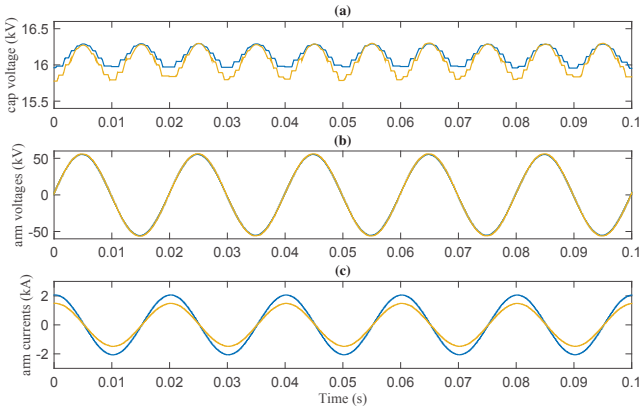

Fig. 12. Simulation results of the proposed strategy with $\angle\overline{i}^{-*} = \frac{\pi}{2}$. (a) cap voltages, (b,c) arm voltages and currents, respectively. Blue: W minimization, yellow: S minimization.

V. Conclusion

In this paper, a novel capacitor-voltage balancing strategy for YYMMC STATCOM operated under unbalanced conditions has been presented. The proposed strategy is based on zero-sequence voltage injection and asymmetric distribution of the line current between the converter arms. It has been shown that the use of the proposed balancing strategy results in significant reduction of the converter energy ratings compared to the classical approach without compromising the semiconductor ratings of the device. The theoretical results have been verified through time-domain simulations.

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