DC-link voltage modulation for individual capacitor voltage balancing in cascaded H-bridge STATCOM at zero current mode

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Keywords

≪Multilevel converters≫, ≪Static Synchronous Compensator (STATCOM)≫, ≪Converter control≫, ≪Modulation strategy≫, ≪Pulse Width Modulation (PWM)≫.

Abstract

Individual capacitor voltage balancing of cascaded H-Bridge converters is one of the challenges in the field of multilevel converters, especially when the converter is operating at zero-current mode. This is due to the fact that the balancing algorithm requires information about the power direction for proper insertion of the different cells of the converter. In case of delta configuration of the phase-legs of the converter, a circulating current inside the delta can be used for balancing purposes. However, this approach can not be used for the star configuration. Focusing on the star, this paper first highlights the issue related to the capacitor voltage balancing at zero-current mode and second proposes a novel method to overcome this problem. The proposed method is based on modulation of the DC-link voltages. The method provides a small amount of current flow during the zero-current mode operation. This current enables the sorting algorithm to provide an appropriate individual balancing. The proposed method is applied to a 7-level star connected cascaded H-Bridge STATCOM modeled in PSCAD and simulation results show the effectiveness of the proposed method in balancing the capacitors voltages when no current is exchanged with the grid. Finally the proposed method is experimentally verified through a down-scaled laboratory set-up.

Introduction

Modular Multilevel Converter (MMC) and Cascaded H-Bridge (CHB) converters are today widely implemented for high-power/high-voltage applications. The output voltage waveform of these converters is synthesized by selecting different voltage levels obtained from the DC-link of each cell.

As the DC-links are constituted by capacitors, the capacitor voltages have to be balanced in order to guarantee a stable operation of the converter. Capacitor voltage balancing is divided into cluster and individual balancing [1]. The focus here is on the individual balancing. For individual balancing several different modulation techniques based on cell sorting algorithm have been proposed in the literature [2],[3]. Sorting algorithm can be implemented through Carrier-Disposition PWM (CD-PWM) [4], Nearest Level Control (NLC) [5, 6, 7], Nearest Vector Control (NVC) [8],[9], Distributed Commutations

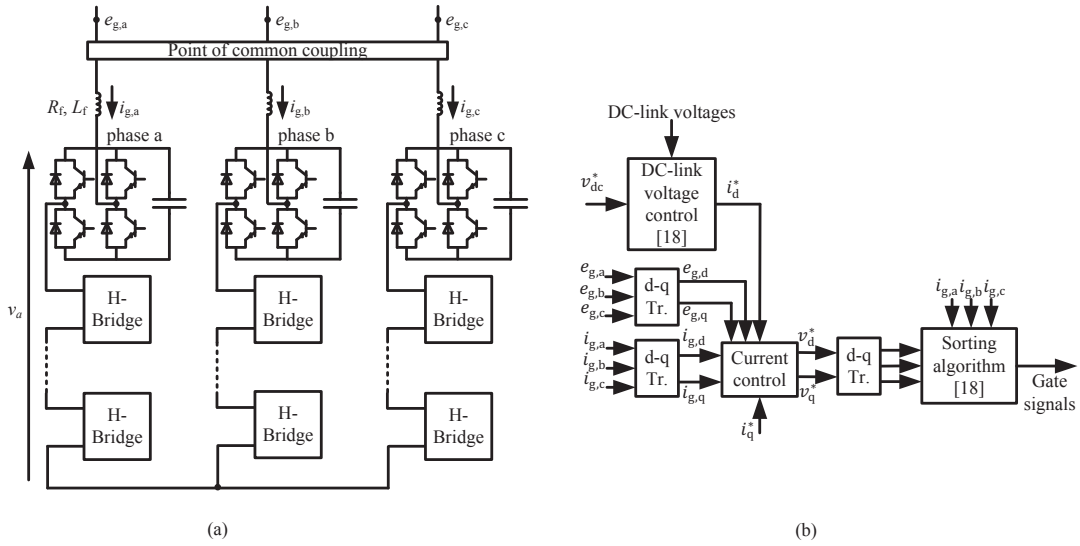

Fig. 1: (a) Star-connected CHB-STATCOM, (b) control block diagram

Modulation (DCM) [10] or predictive sorting algorithm [11]. In order to reduce or completely remove the common mode switching actions, many papers propose different strategies for cell sorting. This has been done in [12] by using Phase-Shifted PWM (PS-PWM) and choosing the cells with highest and lowest voltage only, instead of sorting all the capacitor voltages. The same algorithm with CD-PWM is proposed in [13]. A modification of NLC to remove the common modes is proposed in [14]. Reference [15] proposes three different methods to deal with this problem, which are mainly based on predictions.

Although sorting algorithm is an effective solution for voltage balancing when the converter is exchanging current with the grid, less attention has been paid in the literature for zero current operating mode (no reactive power in exchanged between the converter and the grid). Sorting algorithm needs current sign information to provide a correct sorting pattern. As a consequence, when the exchanging current that flows in the cells is zero, the sorting algorithm is unable to take the correct insertion decision for proper balancing of the DC-link voltages [16]. In practical applications, this is even more problematic when noise is present in the measured current signal.

In configurations such as CHB-delta and MMC, it is possible to force a current that circulates between the phase legs of the converter at zero-current mode without any grid interaction. This circulating current can be used to uniformly distribute the active power among the different cells [17]. However, this solution cannot be implemented in the star case as the circulating current interact with the grid. For this reason, capacitor cells balancing is more challenging in star configuration, especially in case of zero (or more in general, very small) current exchange between the compensator and the grid.

This paper proposes a solution for individual capacitor voltage balancing at zero-current mode. The proposed method is based on modulation of the DC-link voltages where the active power is allowed to be exchanged between the grid and the converter when the converter is operating at zero-current mode with the star configuration. The proposed method is meant for the star configuration, although the same approach can be used for the delta configuration as well. The proposed method is verified via simulation using PSCAD simulation tool and experimental results.

CHB STATCOM and control overview

Figure 1(a) shows the line-diagram of a CHB-STATCOM in star configuration. The control method is implemented in the synchronous dq frame, where the inner loop aims at controlling the converter output while the outer loops are to control the capacitor voltages at each phase and the exchanging reactive power. A Phase Locked Loop (PLL) estimates the transformation angle θ in order to obtain all the dq quantities.

Table I: Circuit parameters in Fig. 1

Rated apparent power	S	120 MVA, 1 pu
Nominal line to line rms voltage	V_s	33 kV, 1 pu
Filter inductance	L	4.3 mH, 0.15 pu
Filter resistor	R	0.136 Ω, 0.015 pu
DC bus voltage of each cell	V_{dc}	10.5 kV, 0.32 pu
Carrier frequency for PWM	f_c	3000 Hz
Grid frequency	f_o	50 Hz
Number of cells per phase	N	3
Capacitor size	C	4mF, 0.087pu

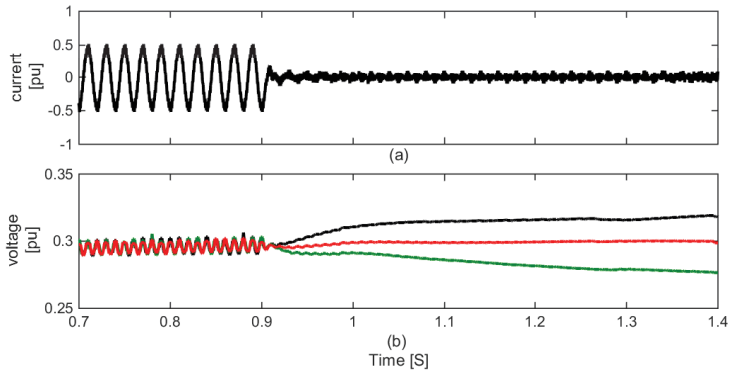

Fig. 2: Conventional sorting algorithm simulation results. (a) Line current, (b) Capacitor voltages

The inner-current control loop [1], based on a PI regulator, generates the reference voltages for each phase. Since the dq transformation is synchronized with the grid voltage, the quadrature component of the current is associate with the reactive power and direct component is associate with the active power. Therefore, the direct component can be used to compensate the STATCOM losses and regulate the DC-link voltage. Detail description of the DC-link voltage control and sorting algorithm can be found in [18]. Figure 1(b) shows the block diagram of the implemented control strategy.

Zero-current operating mode

According with [18], under ideal condition where no current is exchanged between the converter and the grid, the instantaneous current (constituted by the switching ripple only) will change its sign exactly in the middle of the control period. This provides equal charging and discharging areas for the capacitor, leading to a constant DC-link voltage. However, in practical applications this symmetry is typically not achieved, leading to slightly more charging or discharging area. Therefore, the DC-link voltages will not remain constant and diverge from their reference values. The conventional sorting approach will not be able to provide a proper balancing in this case since the sorting approach inserts or bypasses the cells based on the current sign and as the current sign detected in the beginning of the control period is changed during the control period the inserted cells capacitor voltages will deviate from the logic predicted by the sorting approach.

To highlight the problem at zero-current mode, the conventional sorting algorithm is applied to a 7-level star-connected CHB-STATCOM implemented in PSCAD [18]. Table I shows the system parameters selected for the simulation study. Figure 2 shows the obtained simulation results when using the conventional sorting algorithm. Figure 2 (a) shows the line current in phase a while Fig. 2 (b) shows the resulting DC-link voltages in phase a. Similar behavior can be observed for the other phases. All figures are showing the measured quantities in pu. At t=0.9 s, the reactive current is changed from 0.5 pu peak to zero. As it can be observed, the conventional sorting algorithm is not able to provide proper individual cell balancing at zero-current mode.

Proposed DC-link voltage modulation method

Since the problem with the individual DC-link balancing at zero-current mode is being the current very small, the DC-link voltage modulation method attempts to increase the amplitude of the current at zero-current mode by exchanging a small amount of active current with the grid. Active current exchange can be achieved by allowing the capacitor voltages to gently increase and decrease around the desired reference value. To achieve this, a low-amplitude/low-frequency sinusoidal component can be added to the reference DC voltage once the converter operates at zero-current mode, thus forcing a small current exchange between the converter and the grid.

The amplitude of the sinusoidal component should not increase the DC-link voltage beyond the safety margin of the converter. Considering the fundamental component of the current only, with reference to Fig. 1 the converter maximum and minimum voltages are calculated as

$$V = E_{\mathrm{g}} \pm X_{\mathrm{L}} I_{\mathrm{g,rated}} \tag{1}$$

where $I_{\mathrm{g,rated}}$ is the rated current of the converter, E_{g} is the rated grid voltage and X_{L} is the impedance of the filter inductance (filter is assumed to be loss-less). According to (1) the DC-link voltage band for each cell of the star configuration with N number of cells per phase leg is located between a minimum and maximum value as

$$V_{\mathrm{dc}} = \frac{E_{\mathrm{g}} \pm X_{\mathrm{L}} I_{\mathrm{g,rated}}}{N} \tag{2}$$

The DC-link voltage reference can then be written as

$$v^*_{\mathrm{dc}} = \begin{cases} v^*_{\mathrm{dc,0}} + v\cos(2\pi f_{\mathrm{d}} t) & i^*_{\mathrm{q}} = 0 \\ v^*_{\mathrm{dc,n}} & i^*_{\mathrm{q}} \neq 0 \end{cases} \tag{3}$$

where $v\cos(2\pi f_{\mathrm{d}} t)$ is the sinusoidal component with amplitude of v and frequency of f_{d}; the zero-current mode is activated when $i^*_{\mathrm{q}} = 0$. The required DC-link voltage at zero-current mode is equal to the middle of the DC-link voltage band calculated in (2). Therefore, $v^*_{\mathrm{dc,0}}$ and v in (3) should be selected so that the DC-link voltage oscillates between the maximum and the middle of the DC-link voltage band to avoid any over modulation. The voltage $v^*_{\mathrm{dc,n}}$ in (3) can be either designed to the maximum DC-link voltage level or it can be programmed to vary according to (2) [1]. The selection of f_{d} is dependent on the discharging time constant of the DC-link capacitors. It is recommended to select the period of the oscillations, $(1/f_{\mathrm{d}})$, at least one decade larger than the capacitors time constant to ensure that the capacitor voltages will follow the reference voltage. This recommendation also ensures that the DC-link voltage controller will not impact the current control loop since the frequency of the current-control loop bandwidth is typically much larger than f_{d}.

Since the capacitors require small amount of current to change their voltage level, the resulting current caused by this technique is low and the measurement noise and ripple may affect the proper sorting algorithm. Therefore, it is necessary to estimated the current for the sorting algorithm instead of using the measured signal. Since the reactive current during the zero-current mode is very small ($i_{\mathrm{d}} >> i_{\mathrm{q}}$) and assuming a fast and precise current controller ($i^*_{\mathrm{d}} \approx i_{\mathrm{d}}$), it is possible to estimate the current in each phase of the star as

$$\hat{i}_{\mathrm{aY}} = \frac{\sqrt{2}}{\sqrt{3}} i^*_{\mathrm{d}} \cos(\theta) \;\; \hat{i}_{\mathrm{bY}} = \frac{\sqrt{2}}{\sqrt{3}} i^*_{\mathrm{d}} \cos(\theta - \tfrac{2\pi}{3}) \;\; \hat{i}_{\mathrm{cY}} = \frac{\sqrt{2}}{\sqrt{3}} i^*_{\mathrm{d}} \cos(\theta + \tfrac{2\pi}{3}) \tag{4}$$

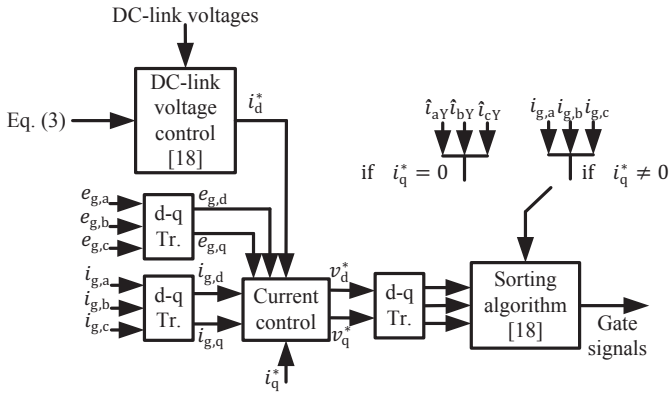

Fig. 3: Overall control block diagram with the proposed control algorithm at zero-current mode

where the factor $\frac{\sqrt{2}}{\sqrt{3}}$ relates to the use of power invariant transformation from dq-reference frame to three-phase system and $\cos(\theta)$ is to make the current in phase with the grid voltage (since the current is mainly active current). Note that i_d^* is determined by the DC-link voltage control loop (see Fig. 1). The current information required for the sorting algorithm can then be written as

$$i = \begin{cases} \text{estimated current from (4)} & i_q^* = 0 \\ \text{measured current} & i_q^* \neq 0 \end{cases} \tag{5}$$

According to (5), once the converter starts to operate at zero-current mode, the estimated currents of (4) are used in the sorting algorithm. For any other operating mode, the measured currents are used. It is of importance to stress that the estimated currents are only used in the sorting algorithm at zero-current mode. The current control will still use the measured currents in the feedback loop. The overall control block diagram with the proposed control algorithm at zero-current mode is shown in Fig. 3.

Simulation results

The proposed DC-link voltage modulation method is applied to the same simulation case study presented in the previous section. Based on the system parameters in Table I and on (3), the DC-link voltage reference is defined as

$$v_{dc}^*[\text{pu}] = \begin{cases} 0.2961 + 0.0239\cos(2\pi 5t) & i_q^* = 0 \\ 0.32 & i_q^* \neq 0 \end{cases} \tag{6}$$

Note that the required DC-link voltage for the zero-current mode is equal to 0.2722 pu. Therefore, to keep the oscillations of the DC-link voltage between 0.2722 and 0.32 pu, $v_{dc,0}^*$ and v in (3) are selected as in (6). 5 Hz is selected for the frequency of the DC-link voltage oscillations.

Figure 4 shows the reactive and active currents together with the corresponding capacitor voltages when using the proposed DC-link voltage modulation technique. As it is shown in Fig. 4 (a), the reference reactive current is set to -1 pu and is changed to 0 and 1 pu at $t = 0.5$ s and $t = 1.5$ s, respectively. Fig. 4 (b) shows the reference active component of the current. It can be observed that once the DC-link modulation technique is activated, i_d^* starts to gently increase and decrease. This leads to a small amount of current flowing into the phase legs of the converter, which is used to provide the appropriate sorting algorithm. Fig. 4 (c) shows the capacitor voltages when the measured currents are used in the sorting algorithm, while Fig. 4 (d) shows the capacitor voltages when using the estimated currents. It can be observed that using the measured current in the sorting algorithm does not result in a perfect individual

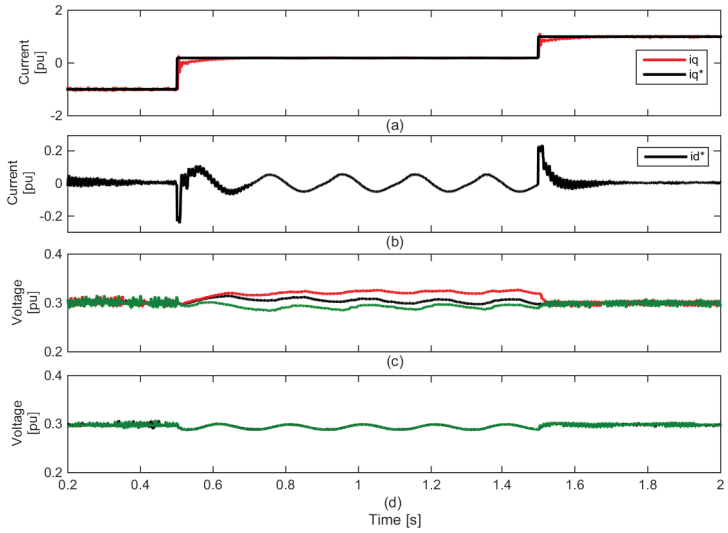

Fig. 4: Simulation results with the proposed method. (a) Reactive component of the current and its reference, (b) Reference active component of the current, (c) Capacitor voltages in phase *a* by using measured current in the sorting algorithm (d) Capacitor voltages in phase *a* by using estimated current in the sorting algorithm

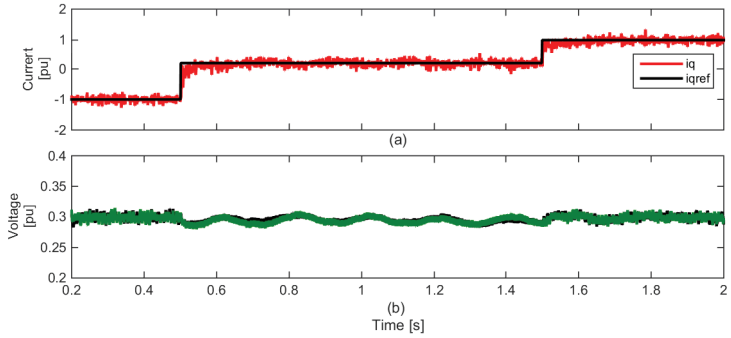

Fig. 5: Simulation results in presence of noise, delay, dead-time and voltage drop. (a) Reference and actual reactive component of the current in phase *a*, (b) Capacitor voltages in phase *a*

balancing while using the estimated currents leads to a proper balancing among the DC-link voltages. This is due to the fact that the resulting current by the proposed method is very small and the current ripples cause problem in appropriate sorting action.

As the current introduced by the proposed method is small, measurement noise can also affect the proper sorting action. To evaluate the robustness of the proposed method, measurement noise (random data with 5% of the nominal values) are added to the measured data. The same simulation as in Fig. 4 is implemented and the results are shown in Fig. 5. It can be observed that proposed method is still able to provide the correct balancing.

The resulting capacitor voltages in presence of grid voltage harmonics are shown in Fig. 6. The reference reactive current is the same as in Fig. 4 (a). It can be observed that in this case the individual balancing fails. Ideally the grid voltage harmonics should not affect the performance of the controller as grid voltage feed-forward is used in the inner current controller [1]. The feed-forward term allows a perfect voltage compensation thus blocking any current harmonic flow into the converter. But since the controller is implemented in discrete time, delays due to discretization and computational time in the control computer result in a phase shift between the actual and feed-forwarded grid voltage. These phase shifts are typically compensated for the fundamental voltage component only, leading to a harmonic current flow between the VSC and the grid.

The presence of the harmonic currents has an impact on the decision taken by the sorting algorithm. This is due to the fact that the harmonics have an amplitude that is higher than the fundamental component.

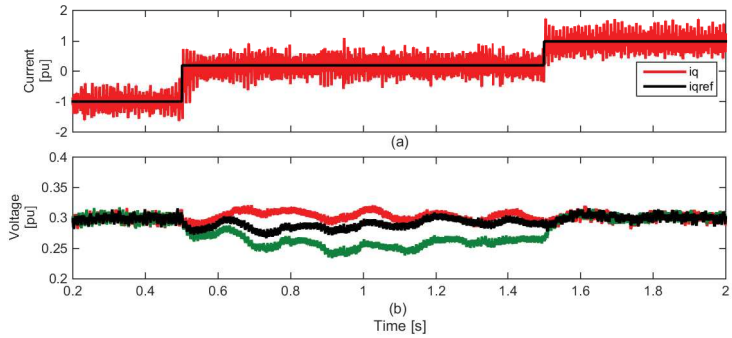

Fig. 6: Simulation results in presence of grid voltage harmonics and DC-link voltage reference of (6). (a) Reference and actual reactive component of the current in phase *a*, (b) capacitor voltages in phase *a*

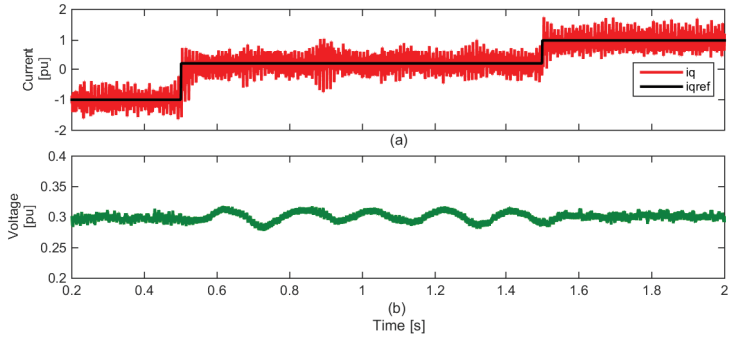

Fig. 7: Simulation results in presence of grid voltage harmonics and DC-link voltage reference of (7). (a) Reference and actual reactive component of the current in phase *a*, (b) capacitor voltages in phase *a*

In order to avoid this effect and at the same time increase the system performance, when the converter is operated under distorted grids the current controller can be improved as suggested in [19], in order to reduce the amplitude of the current harmonics that flow in the converter phase legs. An alternative approach is to simply increase the amplitude of the oscillations introduced in the DC-link voltage and, thereby, increase the amplitude of the fundamental current component. For the considered case, the DC-link voltage reference can be set as

$$v^*_{\mathrm{dc}}[\mathrm{pu}] = \begin{cases} 0.3 + 0.03\cos(2\pi 5t) & i^*_{\mathrm{q}} = 0 \\ 0.32 & i^*_{\mathrm{q}} \neq 0 \end{cases} \tag{7}$$

This indicates that carefulness must be taken in selecting the amplitude of the oscillations when the converter has to be operated under distorted conditions, in order to avoid that the DC-link voltage exceeds the ratings of the cell. Figure 7 shows the simulation results with the new DC-link voltage reference. It can be observed that under this condition the proposed algorithm allows to keep the capacitor voltage balanced.

Experimental results

A down scaled laboratory set-up of the star-connected CHB-STATCOM shown in Fig. 8 with the system parameters reported in Table II is used to verfiy the proposed method. As the parameters of the experimental set-up differ from the simulated model, the reference DC-link voltage is recalculated here. Based on the system parameters, the maximum required DC-link voltage is equal as 0.354 pu. The required DC-link voltage for the zero-current mode is equal to 0.271 pu. Therefore, to keep the oscillations of the DC-link voltage between 0.271 and 0.354 pu, $v^*_{\mathrm{dc},0}$ and v in (3) are chosen to be 0.312 and 0.0006 pu. 5 Hz is selected for the frequency of the DC-link voltage oscillations.

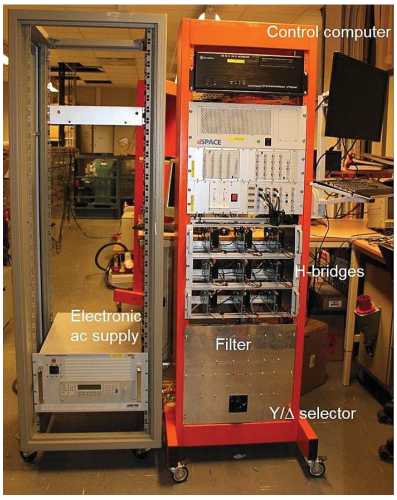

Fig. 8: Picture of the laboratory

Table II: Experimental set-up parameters

Rated apparent power	S	1.5 kVA
Line to line rms voltage	V_s	173.2 V
Filter inductance	L	15 mH
Filter resistor	R	1.4 Ω
DC bus voltage of each cell	V_{dc}	62 V
Carrier frequency for PWM	f_c	3000 Hz
Grid frequency	f_o	50 Hz
Number of cells per phase	N	3
Capacitor size	C	4mF

$$v_{\mathrm{dc}}^{*}[\mathrm{pu}] = \begin{cases} 0.312 + 0.0006\cos(2\pi 5t) & i_{\mathrm{q}}^{*} = 0 \\ 0.354 & i_{\mathrm{q}}^{*} \neq 0 \end{cases} \tag{8}$$

Figure 9 shows the obtained experimental results. Figure 9 (a) shows the reference and actual reactive component of the current. Figure 9 (b) shows the reference active component of the current (i_{d}^{*}). Figure 9 (c) shows the DC-link voltages in phase a when the measured currents are used in the sorting algorithm and Fig. 9 (d) shows the experimental results when the estimated currents are used instead. The reactive current is set to 1 pu until $t = 1.5$ s and is then set to zero from $t = 1.5$ s to $t = 7.5$ s and to -1 pu from $t = 7.5$ s to $t = 8.5$ s. It can be observed that when the converter starts to operate at zero-current mode, the DC-link voltage modulation technique is activated, which leads to small oscillation in i_{d}^{*}. It can also be observed that the sorting algorithm provides a proper balancing when estimated current are used while it fails when using the measured currents, confirming the simulation results.

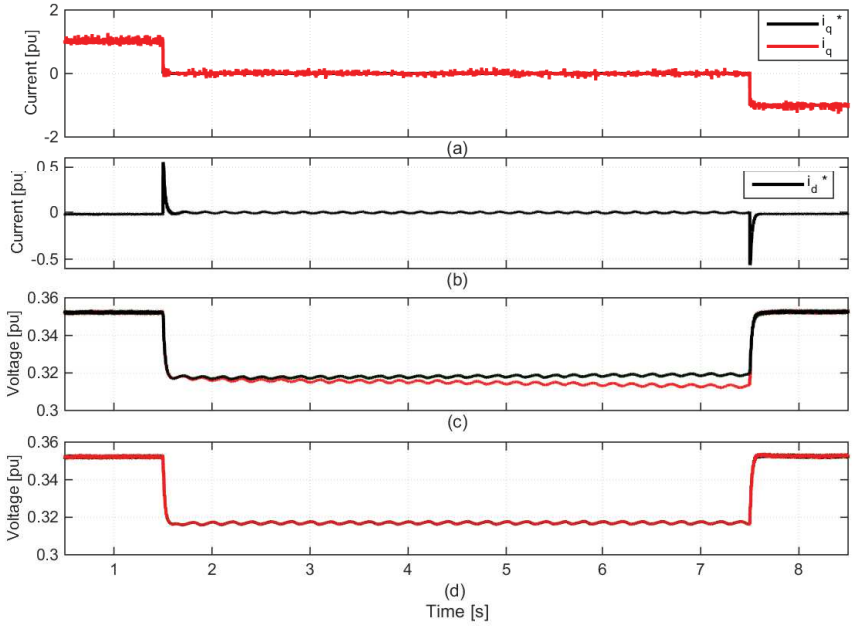

Fig. 9: Experimental results. (a) Reference and actual reactive component of the current, (b) Reference active component of the current, (c) Capacitor voltages in phase a by using measured current in the sorting algorithm, (d) Capacitor voltages in phase a by using estimated current in the sorting algorithm

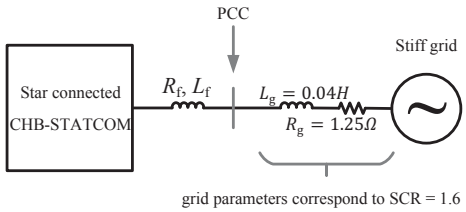

Fig. 10: Equivalent circuit diagram of the star connected CHB-STATCOM connected to the weak grid

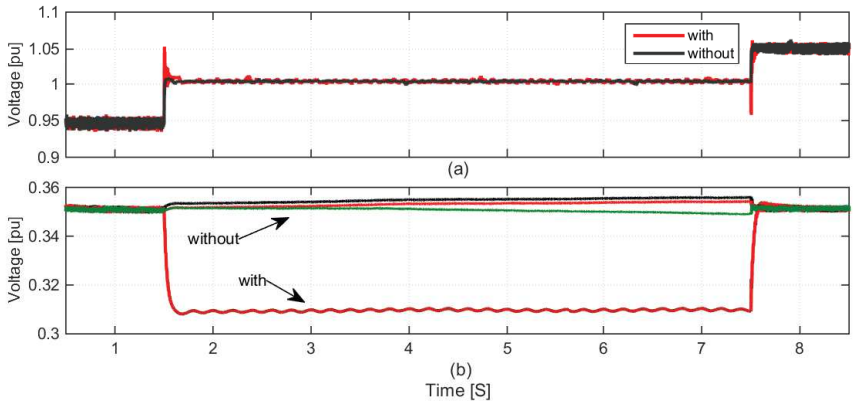

Fig. 11: Experimental results with the weak grid, (a) PCC voltage amplitude with and without the DC-link voltage modulation technique, (b) DC-link voltages in phase a with and without the DC-link voltage modulation technique

The individual balancing with DC-link modulation technique is obtained with a very small value of the amplitude of the oscillations in the DC-link voltages. Consequently the current that flows in the phase legs has very small amplitude and will have negligible impact on the grid voltage. To observe the effect of the DC-link modulation on the grid voltage, the proposed method is experimentally applied to a weak grid set-up as shown in Fig. 10. Inductors with $L_g = 40$ mH are connected in series with the AC Power supply (Fig. 8) at each phase in order to model the grid impedance at weak grid conditions. L_g of 40 mH corresponds to SCR of 1.6 according with the system parameters of Table II. Meanwhile, The reference DC-link voltage of (8) is considered here.

Figure 11 shows the experimental results of the PCC voltage amplitude and capacitor voltages in phase a. The reference reactive current is set to -0.12 pu and then it is changed to zero and 0.12 pu at $t = 1.5$ s and $t = 7.5$ S respectively. Figure 11 (a) shows the grid voltage amplitude, and Fig. 11 (b) shows the capacitor voltages in phase a with and without the DC-link modulation technique. It can be observed that while the DC-link voltage modulation technique is able to provide appropriate balancing among the DC-links under the weak grid condition, it has negligible impact on the PCC voltage amplitude.

Conclusion

In this paper, a method for individual DC-link voltage balancing for star-connected CHB-STATCOM when operated at zero-current mode has been proposed. The investigated method is based on the introduction of a small DC-link voltage modulation that forces a small active power exchange between the converter and the grid. The small resulting active current does not impact the grid voltage at the connection point, even in case of weak grids. Since this current is small and comparable with the current ripple and measurement noise, it is suggested to estimate the current for the sorting process. The proposed method is verified both with a down-scaled laboratory set-up and simulation results. The results show the ability of the proposed method in providing an appropriate individual DC-link voltage balancing at zero-current mode.

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