Electro-thermal Models of Power Modules for Stochastic Optimization of Inverters

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***Abstract*—Stochastic optimization methods are commonly used in the design process of power electronic systems. These require models of crucial parts of the system which are both scalable and computationally efficient. This paper presents thermal models for traction inverter power modules based on scalable chip area that provide high speed of execution and accuracy. The thermal model includes chip-chip interaction, heat spreading and the effects of chip density inside the package. For single-sided modules the temperature error is within 5% for single chip modules and 17% for multichip modules compared to 3D FEM results**

***Index Terms*—Optimzation, power module, thermal model, scalable model.**

I. Introduction

The use of stochastic optimization methods for design of power electronic converters (PEC) is well established [1], [2]. These methods uses a search-space of input parameters to a model (the optimizer) of the power electronic system which evaluates the parameters with respect to one or more design objectives. A large number of evaluations have to be made in order to have a large search-space and high resolution of the input parameters. This puts a high demand on the computational efficiency of the models in order to ensure that the full optimization task can be performed within a reasonable time. At the same time, the models must be accurate enough to ensure that the result is valid in terms of losses and component sizing. For traction applications, power modules are often the chosen package for the semiconductor [3]. Power semiconductors have previously been identified as a major cost driver in power electronic converters and the cost of the semiconductor die itself is the main cost component in the power module. The semiconductor chips is also where the bulk of the losses happen [4]. One important aspect when optimizing a PEC design is to find the correct size and number of chips to put inside a power module package. Chip-area based models of IGBTs and diodes were presented in [5] which include a thermal model. The drawback of this model is that it does not account for chip-chip interaction and the size of the power module. The increased power density of PEC means that these effects are expected to become more important. Additionally, the difficult manufacturing process of SiC wafer means that these chips are often produced with smaller chip areas, (10's of mm^2) than what is possible for Si chips, which can have areas up to ten times larger. For small areas, the effect of heat spreading in the package on the total thermal resistance is relatively larger than for chips with large area (100's of mm^2). This paper presents a scalable one-dimensional thermal model for power modules which addresses these issues and fulfil the requirements regarding accuracy and computational efficiency. An example is provided wherein IGBT and anti-parallel diode chips are sized using losses calculated in motoring and rectifying mode and accounting for thermal coupling between IGBT and diode chips.

II. Loss modelling

The scalable loss models in this paper are based on information available in manufacturer datasheets. For the conduction losses, plots of the voltage drop across the device for currents from zero to twice the rated current ($\mathrm{I_{rated}}$) is typically available. For MOSFET, the voltage drop is estimated using a single resistor, $\mathrm{R_{on}}$, while for IGBTs, the model is complemented with a voltage drop, $\mathrm{V_{on}}$, in series with $\mathrm{R_{on}}$. Temperature coefficients $\mathrm{T_{c,V_{on}}}[\mathrm{V/^\circ C}]$ and $\mathrm{T_{c,R_{on}}}$ $[\Omega/^\circ\mathrm{C}]$ are used to adjust the value of $\mathrm{R_{on}}$ and $\mathrm{V_{on}}$ for junction temperatures ($\mathrm{T_j}$) inbetween those given in the data sheet (usually 25°C ($\mathrm{T_{ref}}$) and 150°C). The temperature coefficients depend on the rated current of the device. By extracting this data from several devices with the same manufacturer, generation and packaging, $\mathrm{R_{on}}$, $\mathrm{V_{on}}$ and are fitted to the $\mathrm{I_{rated}}$ of the device. The on-state voltage drop for a device with rated current ($\mathrm{I_{rated}}$) and device current I is calculated using

$$V_{device} = V_{on} + R_{on} \cdot I \tag{1}$$

$$V_{on} = V_{on,ref(I_{rated})} + T_{c,Von(I_{rated})} \cdot (T_j - T_{ref}) \tag{2}$$

$$R_{on} = R_{on,ref(I_{rated})} + T_{c,Ron(I_{rated})} \cdot (T_j - T_{ref}) \tag{3}$$

For one IGBT of an inverter using sinusoidal PWM modulation the conduction losses are calculated using [6]

$$\begin{aligned} P_{cond} = &\left(\frac{1}{2\pi} + \frac{(m \cdot cos(\phi)}{8}\right) \cdot V_{on} \cdot \hat{I} + \\ &\left(\frac{1}{8} + \frac{m \cdot cos(\phi)}{3\pi}\right) \cdot R_{on} \cdot \hat{I}^2 \end{aligned} \tag{4}$$

and for one diode the losses are calculated using

$$P_{cond} = \left(\frac{1}{2\pi} - \frac{(m \cdot cos(\phi)}{8}\right) \cdot V_{on} \cdot \hat{I} + \left(\frac{1}{8} - \frac{m \cdot cos(\phi)}{3\pi}\right) \cdot R_{on} \cdot \hat{I}^2 \quad (5)$$

The turn-on and turn-off losses have been extracted from data sheets. For each type of device (IGBT, MOSFET, Diode), the switching losses depend on the current rating of the device, the current through the device, the junction temperature and the switching voltage. However, the switching losses are typically only available for $V_{ref} = V_{rated}/2$. By extracting the switching losses from the data sheet, a map of switching losses for various device currents and device current ratings is created. A polynomial fit is used to estimate the switching losses for theoretical devices with current ratings between those that are investigated in this paper. A temperature coefficient, Tc, is used to account for the temperature dependence of the switching loss. It is possible to estimate a linear coefficient since the switching losses are usually given for at least two junction temperatures. K_v is set to 1.4 as advised in [3]. Finally, the switching losses in a device with rated current I_{rated} and device current I switched with frequency f_{sw} is calculated using [3]:

$$P_{sw} = f_{sw} \cdot E_{ref}(I, I_{rated}) \cdot (V_{cc}/V_{ref})^{K_v} \cdot (1 + T_{c,sw} \cdot (T_j - T_{ref})) \quad (6)$$

It should be noted that the switching are highly dependent on the loop inductance, thus the expression above gives only a first approximation of the switching losses of a final design. The total chip-area of a device can be found from the manufacturer or by measurements on a sample.

III. Thermal Modelling

1) Single chip module: The thermal model for a single chip is based on the principle of heat spreading. With this approach, it is assumed that the heat caused by the losses spread evenly from the chip in the subsequent layers, forming a pyramid-shape. The result is a higher thermal conductivity as the heat-conducting area increases with the depth. The angle of the pyramid from the vertical is referred to as the heat spreading angle, θ. The thermal resistance of each layer is the calculated by solving the integral [7]

$$R_{th} = \int_0^d \frac{1}{\lambda(a + 2z \cdot tan(\theta))^2} dz = \frac{1}{(2 \cdot \lambda \cdot tan(\theta)} \left(\frac{1}{a} - \frac{1}{a + 2 \cdot d \cdot tan(\theta)}\right) \quad (7)$$

Where d is the thickness of the layer, a is the side-length of the pyramid shape at the bottom of the previous layer and λ is the thermal conductivity of the layer material. In order to find the heat spreading angle, a model of the power module is built in a FEM software. The steady-state temperature is evaluated at the top and bottom of each layer, centred beneath the chip. The thermal resistance is calculated as

$$R_{th,FEM} = \frac{\Delta T}{P} \quad (8)$$

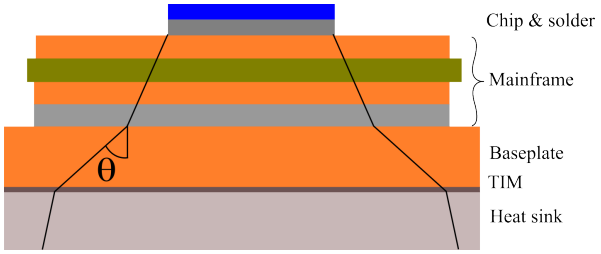

Fig. 1. Side-view of the layers in the single sided module with three different heat spreading angles θ

Where ΔT is the temperature rise and P is the power (losses).

2) Single-sided cooling: A thermal stack consisting of seven layers was built in the FEM software Comsol Multiphysics, see Table I. The steady-state temperature with a single chip has been calculated for several chip areas ranging from 10 to 200 mm^2. Three different heat spreading angles are used for the single sided cooling case. One for the four layers of copper, ceramic, copper and solder (the mainframe), one for the copper baseplate, and one for the heat sink. The chip, chip solder and thermal interface material (TIM) between baseplate and heat sink are assumed to have no heat spreading. A constant power is injected into a single chip and the peak and average steady-state temperatures of the chip are evaluated. For the thermal stack the temperature is evaluated directly below the chip between layers 2 - 3, layers 6 - 7 and layers 8 - 9. The temperature at the bottom of layer 9 is fixed to 0 °C. A reference thermal network with four thermal resistors is then calculated using Eq. 8. The analytical model calculates the first thermal resistor as shown in Eq 9.

$$R_{th1} = \frac{d_{chip}}{\lambda_{chip} \cdot A_{chip}} + \frac{d_{solder}}{\lambda_{solder} \cdot A_{solder}} \quad (9)$$

since the space around the chip and the chip solder is assumed to be a perfect thermal insulator. Thermal resistors 2-4 are calculated by minimizing the difference between thermal resustance calculated using Eq. 8 and Eq. 7.

$$\Delta T/P - \int_0^d \frac{1}{(\lambda(a + 2z \cdot tan(\theta))^2)} dz \quad (10)$$

For θ = [1,89]. This results in three different heat spreading angles θ which depend on the chip area. For the mainframe, heat spreading angle is inverse-proportional to chip area. For the baseplate, the heat spreading angle has no strong correlation to chip area but it is significantly impacted by the thickness of the TIM layer. This is due to the relatively low thermal conductivity of the TIM. For the heat sink, a near linear relationship between chip area and heat spreading angle is found, which is also impacted by the thickness of the TIM layer. The optimal heat spreading angles and the fitted functions can be seen in Fig. 2 and Table III. The fitted functions together with Eq. 7, Eq. 9, and the information in table 1 can then be used to estimate the thermal resistance from junction to heat sink for any chip area between 10 and

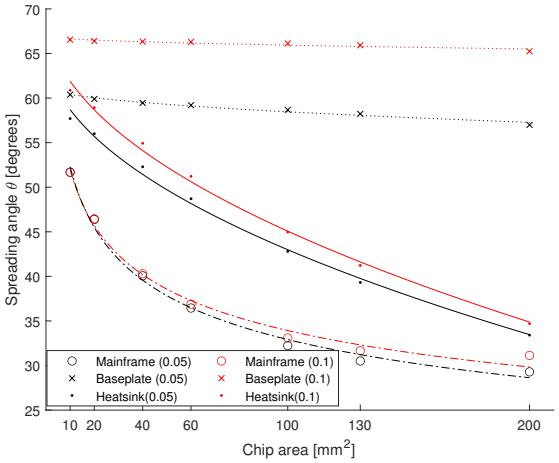

Fig. 2. Optimal heat spreading angles for the single sided module. See Table III for the fitted functions.

TABLE I
LAYER THICKNESS AND THERMAL CONDUCTIVITY (λ), SINGLE-SIDED COOLING

Layer	Material	Thickness [mm]	λ [W/m· K]
1	Chip (Si)	0.1	131
2	Solder	0.05	50
3	Copper	0.3	400
4	Ceramic	0.32	35
5	Copper	0.3	400
6	Solder	0.04	50
7	Baseplate (Cu)	4	400
8	TIM	0.1, 0.05	1
9	Heatsink (Cu)	5	400

200 mm^2. The fitted functions have been selected to allow for extrapolation to longer side-length. This extrapolation is used for multi-chip modules when two or more pyramids intersect. In that case, the heat spreading angle of the longer sides is recalculated using the combined side-lengths in that direction.

To validate this approach for multi-chip modules, up to 5 chips are placed in a row and the distance between them varied between 0.5 and 4 mm, and the peak chip temperature is calculated using FEM. Temperature at the bottom of the heat sink is set to 0 °C and the peak temperature of the most centrally located chip is recorded.

3) Double sided cooling: The modelling approach for the double-sided cooling module is the same as in the single sided case but with heat also dissipating through a material stack above the chip. The baseplate solder and the baseplate (layers 6 and 7) are not included in the double-sided case. There are several approaches to creating the connection between the top side of the chip and the top mainframe, e.g., using copper spacers. In this model, the top side of the chip is assumed to be soldered to the top mainframe, just as it is to the bottom mainframe. The solder at the top side must leave space for gate connections and cannot cover 100% of the top surface of the

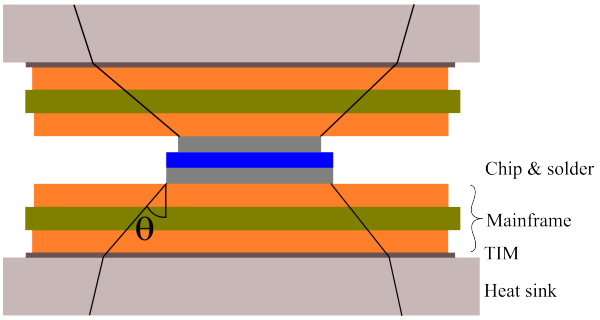

Fig. 3. Side-view of the layers of the double sided module. Heat spreading angles for the top side are adjusted according to the top solder area which is 70% of the chip area.

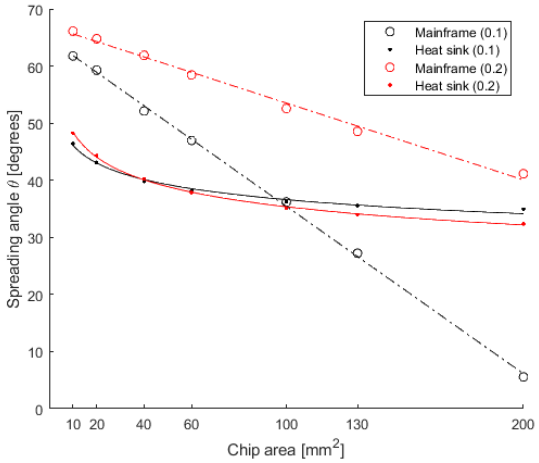

Fig. 4. Optimal heat spreading angles for the double sided module. See Table III for the fitted functions.

chip. It is assumed that 70% of the surface can be soldered to the time mainframe and thus conduct heat. The parts of the chip that are not covered by solder are thermally insulated from the top side in the FEA model. Thus, heat spreading angle for the top side is calculated using 70% of the chip area. The thermal resistance of the chip is divided between the top and bottom side. Heat spreading angles for a single chip are found using the same approach as in the single-sided case. Only two heat spreading angles are used, one for the mainframe and one for the heat sink. The heat spreading angles are found for the bottom side where the 100% of the chip is connected to the mainframe through the solder. Optimal heat spreading angles for the bottom side can be found in Fig. 4. The heat spreading angle for the top side is adjusted to the area of the top chip solder, using the fitted functions. Due to the steep slope of the fitted functions, extrapolation of the heat spreading angle in case of collision between two pyramids is not possible and the original heat spreading angle is used instead. The thermal conductivity of the TIM layer is increased to 6 $\mathrm{W/m \cdot K}$ to represent a high-performance TIM.

4) Multichip modules: When two or more chips are placed nearby in the power module, thermal p performance of each

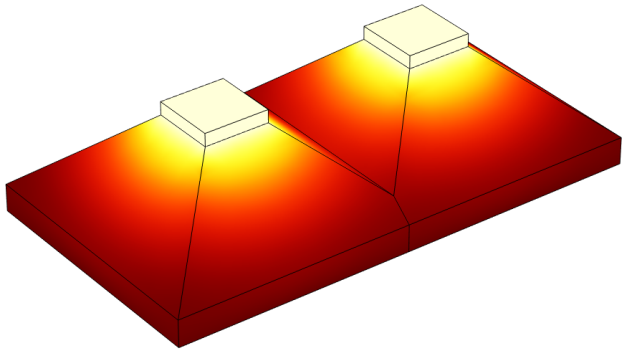

Fig. 5. Illustration of two intersecting heat conducting pyramids, forming a network with three thermal resistors.

chip is worsened. To capture this, thermal resistance of each chip is calculated up until the point where the pyramid-shapes intersect, using equation 7. After that point, the heat conducting areas of each pyramid are combined and the heat fluxes from the chips are summed. The new heat-conducting pyramid has a non-square base and continues to grow until it reaches the bottom of the heat sink. This is illustrated in Fig. 5. The thermal resistance from the point of collision is calculated using

$$R_{th} = \int \frac{1}{\lambda \cdot ((l + 2 \cdot tan(\theta)) \cdot (w + 2 \cdot tan(\theta))} \qquad (11)$$

where l and w are the length and width of the pyramid. Equation (11) is evaluated numerically.

5) IGBT-Diode pairs: An IGBT has an anti-parallel diode chip which is mounted near the IGBT chip. The diode will usually have lower losses and smaller size than the IGBT. In order to investigate the effect of thermal coupling between the IGBT and diode chips, simulations were preformed on the single-sided module where a row of chips representing the diodes is placed next to a row representing the IGBTs. 50W of power is injected in each of the diode chips and the area is set to ½ times the area of the IGBTs. IGBT-diode distance and IGBT-IGBT distance is varied independently between 0.5 and 4 mm, see Fig. 6. Simulations were preformed for 1-5 IGBTs with the same number of anti-parallel diodes. Calculation of the heat-spreading pyramids is more complicated than in the case with only transistors, since there are up to three intersection points where heat spreading pyramids intersect.

IV. Results

Figure 8 shows the thermal resistance from chip to heatsink of single-sided power modules with 1-5 20 mm^2 transistors mounted in a row with a distance of 2 mm between them. The figure shows that large errors in estimated chip temperature can be expected if the thermal resistance of one chip is used for multi-chip modules. Figure 9 shows the error of the model

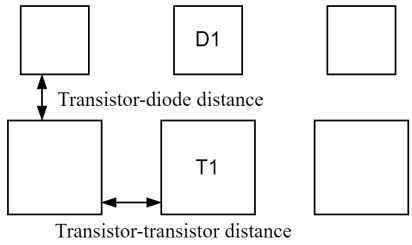

Fig. 6. Chip placement for IGBT-diode pairs.

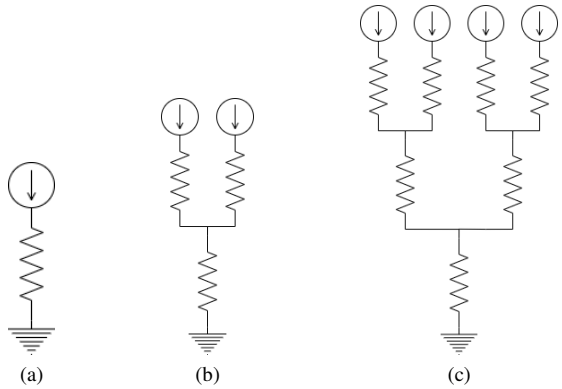

Fig. 7. Equivalent thermal network of power modules with (a) single chip, (b) two transistors, and (c) two transistors and two diodes.

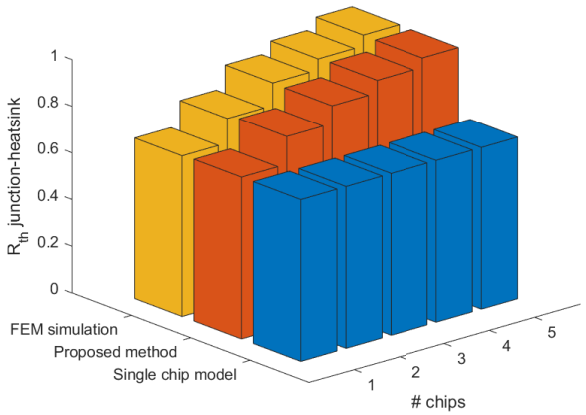

Fig. 8. Comparison of thermal from junction to heat sink for multi-chip modules, single sided cooling with 0.1 mm TIM, 20 mm^2 chip area and 2 mm space between chips. No diode is used in this example.

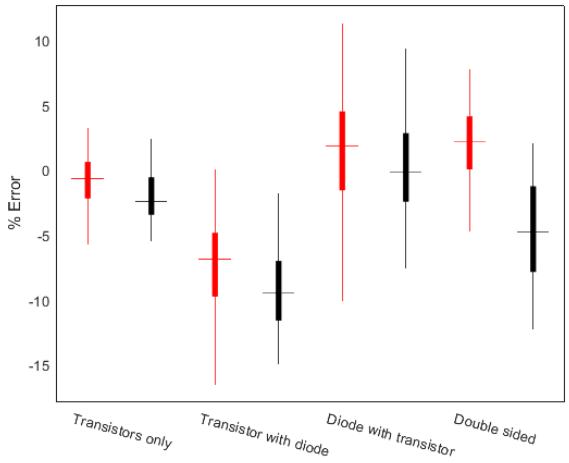

Fig. 9. Boxplot showing the error in estimation of peak chip temperature using the proposed method compared to FEM simulation, with thicker (red) and thinner(black) TIM layers. The thick lines represents the 25th and 75th percentiles and the horizontal lines represent the average error.

compared to FEM simulation. A negative percentage means that the proposed model results in a lower temperature than FEM simulation. Adding anti-parallel diodes to the model increases the maximum error substantially. The error with double sided cooling (no diodes are used in this case) is also larger than for single sided cooling. Simulation time on a modern laptop with 16 GB RAM is on the order of tens of seconds using Comsol Multiphysics while the proposed method takes a few μs.

V. Example application

In this section, an example is provided to illustrate the benefits of the proposed model compared to the conventional model using the thermal conductivity from a single chip (i.e. without considering thermal coupling). The example concerns correct sizing of IGBT and diode chips for a power module with single sided cooling. The parameters of the power module and the operating point are shown in Table II. As the size of the power module is limited, the heat spreading angle is set to 0 when the pyramid shape reaches the power module edge.

As a baseline, the size of the chips is optimized for the maximum allowed junction temperature using the proposed method. The same chip area and losses are then used to estimate the temperature rise from heat sink to junction using the conventional single chip model and 3D FEM, the last method being the most accurate but also the most computationally expensive and thus not well suited for stochastic optimization. Figure 10 shows the temperature rise from heat sink to junction for the three methods. The lower temperature of the single chip model suggests that smaller chips could be used. However, doing so would result in overheating the chips. It can also be seen that the single chip model predicts much lower temperature for the device that is less loaded (i.e. the diode in motoring mode). This will result in underestimation

TABLE II
Parameters used for chip sizing in the application example

Phase current	300 A rms
DC line voltage	400 V
Modulation index	0.9
Power factor for IGBT sizing	0.95
Power factor for diode sizing	-0.95
$T_{j,max}$	150 °C
Heat transfer coefficient	5 $\mathrm{kW/m^2}$
Ambient temperature	60 °C
Cooling	Single-sided
TIM	0.1 mm, $\lambda = 1W/m^2K$
Power module measurements	50 x 30 mm
Number of IGBT chips	3
Number of diode chips	3
Space between IGBT chips	3 mm
Space between IGBT and diode chips	3 mm
Resulting IGBT area per chip	53.7 $\mathrm{mm^2}$
Resulting diode area per chip	30.1 $\mathrm{mm^2}$

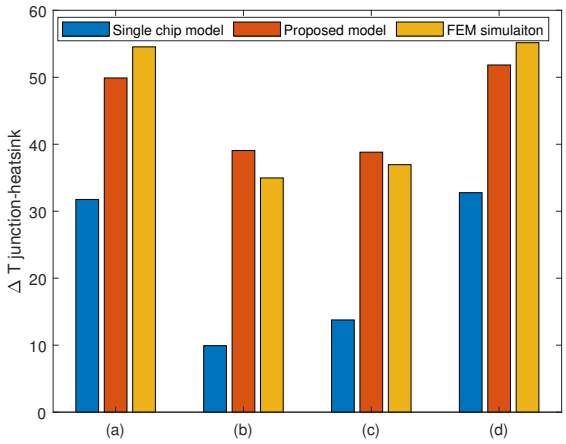

Fig. 10. Temperature rise from heat sink to junction for (a) IGBT with PF = 0.95, (b) diode with PF = 0.95, (c) IGBT with PF = -0.95, (d) diode with PF = -0.95.

of the losses and thus a slight overestimation of the overall efficiency. On the other hand, the proposed method estimates temperatures which are significantly closer to those obtained using FEM while being several orders of magnitude faster to compute. This makes the proposed method a suitable choice for applications that require evaluation of large numbers of layouts.

VI. Conclusion

A scalable thermal model for power modules has been presented in this paper. By combining the model with loss models linked to chip area the proposed method can be used for chip sizing in applications where there is a high demand on computational efficiency, such as stochastic optimization. Estimates of thermal resistance is within 17% for the modelled layouts. The paper shows that it is possible to estimate the effect of thermal coupling between nearby chips by using the principle of a heat spreading angle. The heat spreading angle

TABLE III
FITTED FUNCTIONS FOR HEAT SPREADING ANGLE DEPENDENCE ON CHIP AREA $[mm^2]$

Cooling sides	TIM thickness	function	a	b
Single-sided mainframe	0.1 mm	$a * x^b$	79.58	-0.3703
Single-sided mainframe	0.05 mm	$a * x^b$	83.08	-0.4021
Single-sided baseplate	0.1 mm	$a * x + b$	-0.1034	66.97
Single-sided baseplate	0.05 mm	$a * x + b$	-0.286	61.32
Single-sided heat sink	0.1 mm	$a * x + b$	-2.461	69.68
Single-sided heat sink	0.05 mm	$a * x + b$	-2.299	65.98
Double-sided mainframe	0.1 mm	$a * x + b$	-0.2932	64.76
Double-sided mainframe	0.2 mm	$a * x + b$	-0.1346	66.98
Double-sided heat sink	0.1 mm	$a * x^b$	58.12	-0.1004
Double-sided heat sink	0.2 mm	$a * x^b$	66.28	-0.1364

is highly dependent on the thickness and conductivity of the TIM layer.

The use of the proposed model shows a significant improvement in accuracy of temperature estimation over the conventional single chip model that is widely used in the literature, while having an execution time several orders of magnitude shorter than 3D FEM. This allows for a more precise sizing of semiconductor devices by taking into account the thermal coupling between the different chips inside the power module as well as the edge effect.

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